Silicon nitride gate dielectric for top-gated carbon nanotube field effect transistors

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(Received 3 June 2004; accepted 4 October 2004; published 10 December 2004)

We develop and demonstrate a process to fabricate top-gated carbon nanotube transistors using silicon nitride as the gate dielectric. *I-V* curves of these silicon nitride gated nanotube transistors are measured. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1824048]

I. INTRODUCTION

Of the various possible geometries for carbon nanotube field effect transistors (CNTFETs), top-gated CNTFETs (as shown in Fig. 1) are the most promising because they allow local gate biasing at low voltage, possible high speed switching,[1] and high density of integration. To date, two kinds of oxide thin films have been developed as gate dielectrics for CNTFETs: The first method[2] uses low temperature oxidation to deposit SiO_2 thin film from SiH_4 and O_2 at 300 °C; the other method[3] implements atomic layer deposition (ALD) to deposit ZrO_2 from $ZrCl_4$ precursor and H_2O oxidizer in a N_2 carrier gas. Other oxides such as HfO_2 (Ref. 4) and TiO_2 (Ref. 5) also have been investigated. Since nanotube transistors are known to be effected by the presence of oxygen,[6,7] and because they are susceptible to burning in an oxygen rich environment at elevated temperatures, investigations of oxygen free dielectrics may be of interest. In this work, we present and demonstrate a process to fabricate silicon nitride top-gated nanotube transistors, and present preliminary device results.

Silicon nitride has been intensively investigated for decades as an alternative to SiO_2 gate dielectric due to its relatively higher dielectric constant ($\kappa=7.8$),[8] strong resistance to impurity diffusion and compatibility with conventional complimentary metal-oxide semiconductor (CMOS) processes. Numerous attempts to develop the chemical vapor deposition (CVD) silicon nitride into a viable gate dielectric directly for CMOS have encountered two major difficulties: (1) poor nitride/Si interface properties and (2) high density of bulk traps in silicon nitride. The first difficulty does not apply to CNTFETs in that only the CNTs would be in direct contact with silicon nitride, and it is expected that the fully bonded CNT (with no dangling bonds) would not give rise to nitride/CNT interface states. The second drawback is far more complicated but should be solvable as emerging thin film deposition techniques such as ALD[9] and jet vapor deposition (JVD)[8] have shown very encouraging results. Additionally, the nitride/oxide stack dielectrics have shown promising results for continued downscaling of CMOS devices.[10,11]

Most importantly, the advantage of silicon nitride over oxide as gate dielectric for CNTFETs lies in the chemical process that is benign to CNTs. Silicon nitride thin film is usually deposited from a mixture of reactant gases of SiH_4 and N_2 or NH_3. Film formation takes place as a result of reactions between a number of excited species such as excited molecules of NH_3 (or N_2) and SiH_4, NH, NH_2 (radicals), and unexcited molecules and their condensation on the substrate.[12] The overall reaction is

$$SiH_4 + NH_3(\text{or } N_2) \rightarrow Si_3N_4.$$

Oxygen associated species are absent from the Si_3N_4 deposition process and ammonia and its derivatives should be more benign to CNTs as shown in Ref. 13, where NH_3 excited by plasma is found to play a crucial catalytic role to promote the growth of CNTs.

In this work, we examine the chemical compatibility of silicon nitride with CNTFET fabrication process. Silicon nitride was deposited using a plasma enhanced chemical vapor deposition (PECVD) system and silicon dioxide was also deposited using the same equipment for direct comparison. We demonstrate the viability of using silicon nitride as gate dielectric for CNTFETs. The goal of this article is to investigate the compatibility of silicon nitride with CNTFETs by using the most commonly available technique—PECVD. More sophisticated techniques such as JVD and ALD should improve the quality of our devices.

II. DEVICE FABRICATION

A. Nanotube growth

The CNTs were grown from lithographically patterned nanoparticle catalyst sites using CVD.[14] The nanotube growth procedure and recipes are described in detail in Ref. 15. The diameter of CNTs grown this way ranges from 1 to 4 nm as measured with an atomic force microscope (Digital Instruments, Multimode, Santa Barbara, CA).

B. Source-drain contacts

A scanning electron microscopy (SEM) (Hitachi 4700) was used to locate the CNTs and the catalyst pattern was used as an alignment marker to align metal contacts to the CNTs. Source and drain electrodes made of Ti/Au thin film was achieved by conventional optical lithography and elec-

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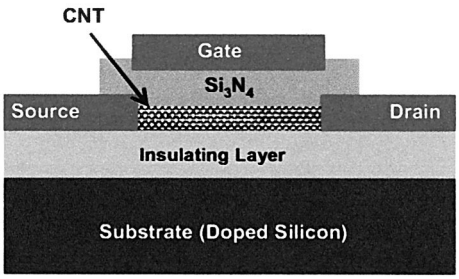

FIG. 1. Schematic cross-section view of top-gate nanotube transistor.

tron beam evaporation. The scaling limit of the length of the CNTs from source to drain was only subject to the resolution of the lithography system. After depositing source and drain electrodes, a SEM was employed again to identify the number of CNTs in between.

C. Silicon nitride deposition

Silicon nitride thin film was deposited from SiH_4 and NH_3 in a high purity N_2 carrier gas at 225 °C by PECVD (Plasma-Therm Model 790). The software interface of Plasmas-Therm Model 790 allowed easy control of the thickness of gate dielectric. For comparison, a SiO_2 thin film was also deposited on similar samples from SiH_4 and N_2O under the same conditions.

The exact film thickness was determined by an ellipsometer. Reactive ion etching, also built on the Plasma-Therm Model 790, was then utilized for opening holes in the silicon nitride to the source and drain electrodes. The gate electrode was defined using optical lithography and the appropriate gate length was also limited by the resolution of the lithography system. The schematic fabrication sequence is depicted in Fig. 2.

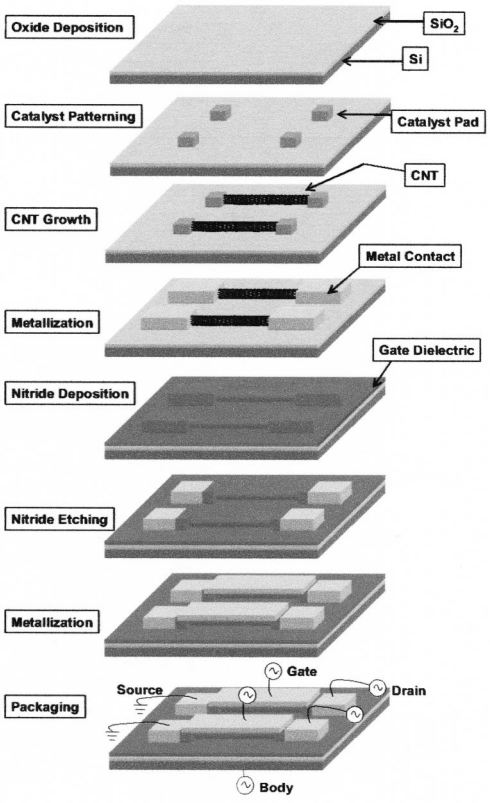

FIG. 2. Detailed processing steps (not to scale).

III. RESULTS AND DISCUSION

Electrical transport measurements were carried out at room temperature and 4 K on over 50 Si_3N_4/CNT and SiO_2/CNT transistors obtained from devices fabricated during various CNT growth and dielectric thin film deposition runs. We first discuss the SiO_2/CNT transistors. For these devices, the source-drain electrical conduction was zero. This is not surprising considering the fact that various oxygen related species prevalent during the deposition of SiO_2 are radicals or excited molecules, which readily destroy CNTs by chemical reaction.[3] This supports our motivation for investigating an oxygen-free dielectric material.

We next discuss the Si_3N_4/CNT transistors. Of the devices studied, about 60% showed room temperature conduction (at low source-drain bias) from source to drain, typically of the order a few μS. Of these, the yield of devices which showed response to the top gate voltage was about 10%. Our work represents top-gated nanotube transistors fabricated purely with optical lithography. Because of the resolution limit of optical lithography and the density of our CVD grown tubes, typically, the number of the nanotubes underate is 1–3. Typically if one CNT is metallic, then the gated devices do not turn totally "off." This issue will be clarified in future work with electron-beam lithography defined devices, where it will be more straightforward to contact individual nanotubes.

The depletion curve at room temperature shows only weak dependence on top-gate voltage, again probably due to the presence of metallic nanotubes under the gate. In addition, the room temperature depletion curve exhibits some hysteresis. We attribute this to electron traps, which are typical of nitride dielectrics. In order to further investigate the transport properties, we measured the source-drain *I-V* curves at low temperatures, where the metallic background disappeared and the response to the gate voltage was much stronger. The low temperature also freezes out the charge traps and thus minimizes the hysteresis.

Figure 3 shows an *I-V* curve measured at 4 K for a variety of top-gate voltages. *I-V* curves were taken continuously by sweeping the gate voltage V_g from +1.0 to −1.0 V ($\Delta V_g = 0.1$ *V*). The gate-modulated conductance increases consistently with decreasing V_g. On any given device, these results are quantitatively reproducible within a given cooldown cycle. After thermal cycling, the results are qualitatively similar. Our findings indicate that the nanotube operates in depletion mode, i.e., the threshold voltage is above +1 V. This indicates that the nanotubes may be *p* doped at some point during the deposition process. Since a detailed micro-

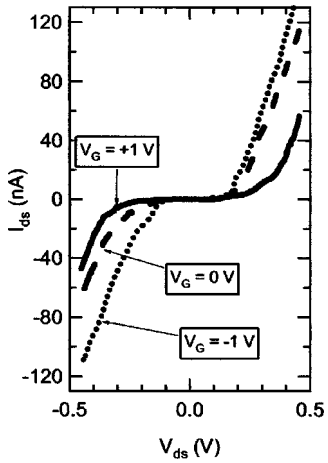

FIG. 3. *I-V* characteristics of a top-gated CNTFET using silicon nitride gate dielectric (dielectric thickness 50 nm; gate length 10 μm; T=4 K).

scopic theory of the interaction of CNTs with Si_3N_4 is not available, the mechanism of *p* doping is currently an open question.

We next discuss the low conductance at the origin, i.e., low source-drain voltages. Since the temperature is low, even a small Schottky barrier ($\sim$10 meV) at the metal-nanotube contact could account for the observed gap in current around the origin. This indicates that our top-gated SiN/CNT transistors are consistent with the Schottky barrier model for transistor action in carbon nanotubes.[16] Similar behavior was observed in back-gated CNT devices by Martel *et al.*[17] in 1.5 μm long nanotubes at 4 K, and by Zhou *et al.*[18] in 3 μm long nanotubes at 4 K. Ours is an observation at 4 K in top-gated nanotube devices.

IV. CONCLUSION

In conclusion, we have developed and tested a process to fabricate carbon nanotube top-gate field effect transistors using silicon nitride as the gate dielectric. Our work represents a demonstration of gating a nanotube with an oxygen-free dielectric. Considering our dielectric thickness of 50 nm and gate length of 10 μm, there is still significant room for improvement. For example, more advanced thin film deposition techniques such as ALD and JVD instead of PECVD could be used to fabricate thinner dielectrics. In addition, shorter gate-length devices may achieve higher transconductance. By careful electron beam lithography in future experiments we should be able to produce devices with only one nanotube, hence improve the on/off ratio, and measure the room temperature characteristics such as the subthreshold slope, depletion curve, and maximum on current.

ACKNOWLEDGMENTS

This work was supported by the Army Research Office (Grant No. DAAD19-02-1-0387), the Office of the Naval Research (Grant No. N00014-02-1-0456), and DARPA/SSC SD (Grant No. N66001-03-1-8914).

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