

1	2	3	4	Total
/25	/25	/25	/25	/100

**THREE PROBLEMS TOTAL.**

**DO NOT BEGIN THE EXAM  
UNTIL YOU ARE TOLD TO  
DO SO.**

**PROBLEM ONE:**

Short answer.

- A) An average hole drift velocity of  $10^3$  cm/sec results when 2 V is applied across a 1-cm-long semiconductor bar. What is the hole mobility inside the bar?

$$\mathcal{E} = \text{electric field} = 2V / 1\text{cm} = 2 \text{ V/cm} \quad (3\text{pts})$$

$$V_d = \mu_p \mathcal{E} \Rightarrow \mu_p = V_d / \mathcal{E} = 10^3 / 2 = 5 \times 10^2 \text{ cm}^2/\text{V}\cdot\text{sec} \quad (3\text{pts})$$

- B) Name the two dominant carrier *scattering* mechanisms in nondegenerately doped semiconductors of device quality.

(1) *Lattice scattering: collisions with thermally agitated lattice atoms.* (3pts)

(2) *Ionized impurity scattering.* (3pts)

- C) For a given semiconductor the carrier mobilities in intrinsic material are (choose one: higher than, lower than, the same as) those in heavily doped material. Briefly explain why the mobilities in intrinsic material are (chosen answer) those in heavily doped material.

*The carrier motilities in intrinsic material are higher than those in heavily doped material, because there are high numbers of ionized impurities in the heavily doped materials causing more ionized impurity scattering, hence results in systematical decrease in the carrier motilities.*

*(2pts for stating lower; 5pts for correct explanation)*

- D) The electron mobility in a silicon sample is determined to be  $1300 \text{ cm}^2/\text{V}\cdot\text{sec}$  at room temperature. What is the electron diffusion coefficient?

$$\mu_n = 1300 \text{ cm}^2/\text{V}\cdot\text{sec}$$

Using Einstein relationship:

$$D_n = \mu_n \cdot (KT/q) = 1300 \times 0.026 = 33.8 \text{ cm}^2/\text{sec}$$

*(3pts for correct equation,*

*5pts for correct equation and correct substitution*

*6pts for correct equation, correct substitution, and correct answer)*

**PROBLEM TWO:**

A) For the diode below, note that  $E_v(-\infty) = E_c(+\infty)$ . What is the magnitude of the reverse bias voltage  $V_A$  applied to the diode? Explain how you arrived at your answer.

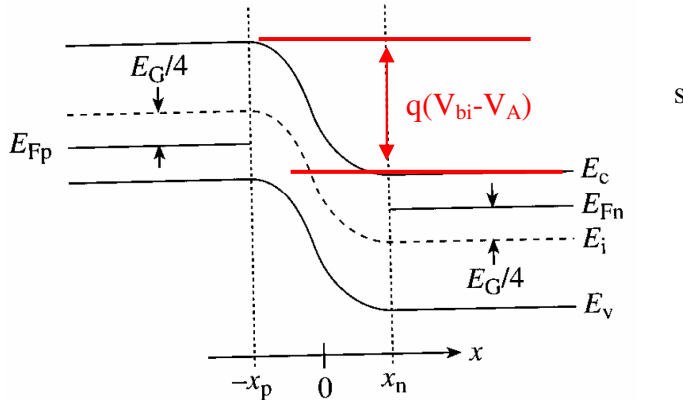
Explanation:

$$E_{Fp} - E_{Fn} = qV_A \quad (2pts)$$

$$E_{Fp} - E_{Fn} = (E_{Fp} - E_i) - (E_{Fn} - E_i) = (-E_G/4) - (E_G/4) = -E_G / 2 = qV_A \quad (2pts)$$

$$\therefore V_A = -E_G / 2q \quad (V) \quad (1pts)$$

B) Determine  $V_{bi}$ , the built-in voltage.



Since  $E_v(-\infty) = E_c(+\infty)$ ,  $q(V_{bi} - V_A) = E_G \quad (2pts)$

$$\therefore V_{bi} = (E_G / q) + V_A = E_G / 2q \quad (V) \quad (1pt \text{ for } E_G/2, \text{ i.e., without the "q"}; \quad 2pts \text{ for correct answer})$$

C) Complete the tables below by indicating the polarity (+ or -) of the input and output voltages associated with each of the four biasing modes.

(a) *npn*

Mode	$V_{EB}$	$V_{CB}$
Active	+	-
Inverted	-	+
Saturation	+	+
Cutoff	-	-

(b) *npn*

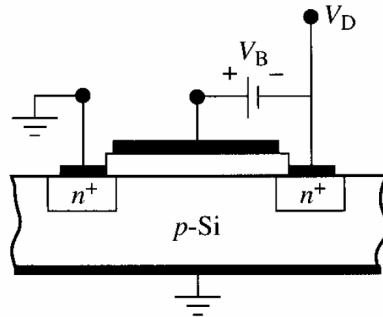
Mode	$V_{BE}$	$V_{BC}$
Active	+	-
Inverted	-	+
Saturation	+	+
Cutoff	-	-

(1pts for each correct polarity)

**PROBLEM THREE:**

Suppose a battery  $V_B \geq 0$  is connected between the gate and drain of an ideal  $n$ -channel MOSFET as pictured in Fig. P17.9. Using the square-law results,

- (a) Sketch  $I_D$  versus  $V_D$  ( $V_D \geq 0$ ) if  $V_B = V_T/2$ ;  
 (b) Sketch  $I_D$  versus  $V_D$  ( $V_D \geq 0$ ) if  $V_B = 2V_T$ .

**Figure P17.9**

(a)  $V_B = V_T/2 = V_G - V_D \Rightarrow V_G = (V_T/2) + V_D$

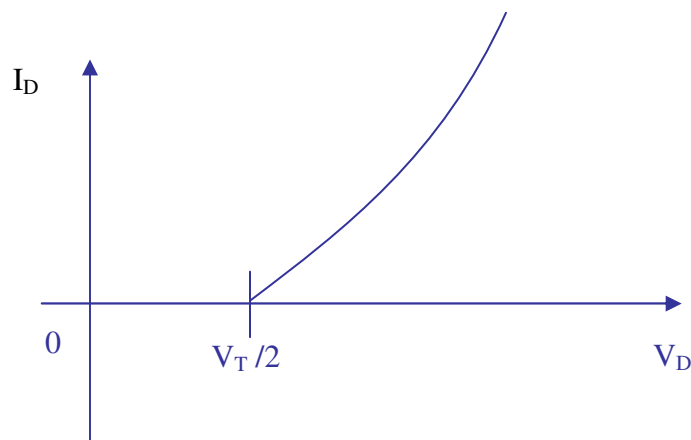
For  $0 \leq V_G < V_T$ , i.e.,  $(-V_T/2) \leq V_D < (V_T/2)$ ,

$\Rightarrow$  The nmos is in the cutoff region,  $I_D = 0$ .

For  $V_D \geq (V_T/2)$ ,  $V_{GD} = (V_T/2) < V_T$

$\Rightarrow$  The nmos is in the saturation region.

$\Rightarrow I_D \propto (V_{GS} - V_T)^2 = [(V_T/2) + V_D - V_T]^2 = [V_D - (V_T/2)]^2$



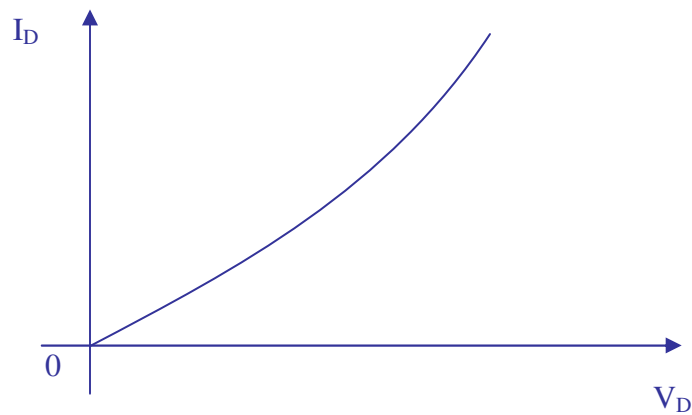
*(-5pts for graph showing current saturation  
 -2pts for not showing current = 0 when  $V_D < V_T$ ,  
 -10pts for other incorrect plots)*

$$(b) \quad V_B = 2V_T = V_G - V_D \quad \Rightarrow \quad V_G = 2V_T + V_D$$

For  $0 \leq V_G < V_T$ , i.e.,  $V_D < (-V_T)$ , the nmos is in the cutoff region,  $I_D = 0$ .

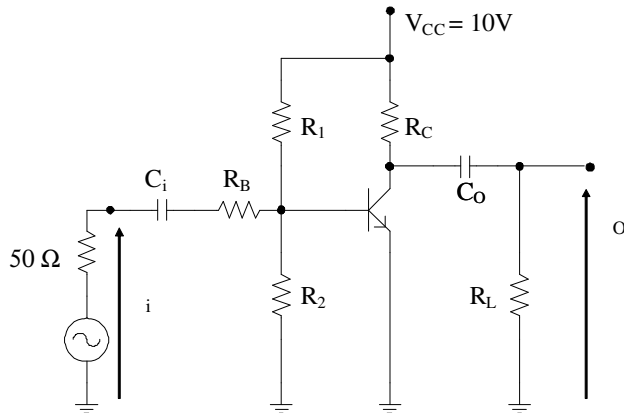
For  $V_D \geq (-V_T / 2)$ ,  $V_{GD} = (2V_T) > V_T$ , the nmos is in the triode region.

$$\begin{aligned} I_D &\propto [(V_{GS} - V_T)V_{DS} - V_{DS}^2/2] \\ &= [(2V_T + V_D - V_T) V_D - V_D^2/2] \\ &= [V_T V_D + V_D^2 - V_D^2/2] \\ &= [V_T V_D + V_D^2/2] \end{aligned}$$



*(-5pts for graph showing current saturation  
-2pts for not showing current =0 when  $V_D = 0$ ,  
-10pts for other incorrect plots)*

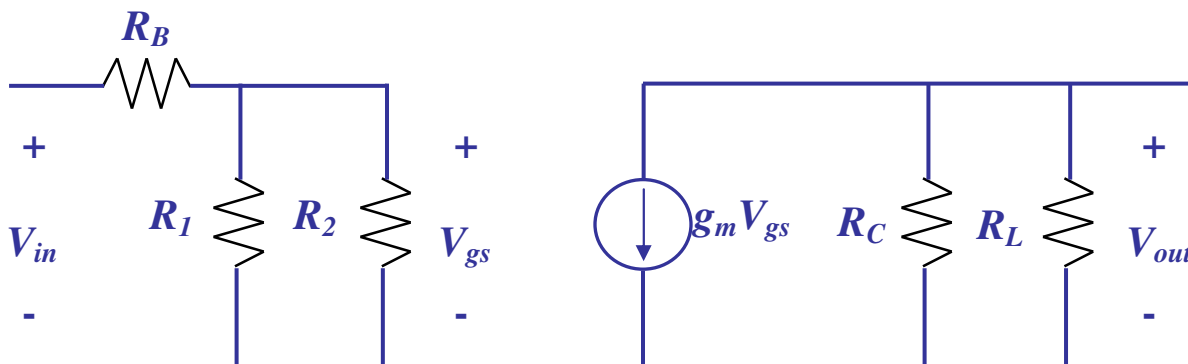
**PROBLEM FOUR:**



The figure above is the amplifier built for the EECS170LA.

A) Assume the transistor is a MOSFET. Using the square-law theory, find the small signal gain in terms of  $R_1$ ,  $R_2$ ,  $R_B$ ,  $R_C$ , and the transistor properties:  $Z$  (width),  $\mu$  (effective mobility),  $V_G$ ,  $V_T$ ,  $C_o$ . (Assume  $R_L$  is very large). Ignore  $C_{GS}$ . Do this by putting in the hybrid  $\pi$  model for the MOSFET and the transconductance  $g_m$  from the square law theory in terms of the transistor gate width  $Z$ , mobility  $\mu$ ,  $C_o$ ,  $V_G$ , and  $V_T$ .

Small signal model:



$$V_{gs} = [(R_1 \parallel R_2) / ((R_1 \parallel R_2) + R_B)] \cdot V_{in}$$

*(5 pts for correct  $V_{gs}$  expression)*

$$V_{out} = -g_m V_{gs} (R_L \parallel R_C)$$

*(5 pts for correct  $V_{out}$  expression)*

$$\text{Gain} = V_{\text{out}} / V_{\text{in}} = -g_m (R_L \parallel R_C) [(R_1 \parallel R_2) / ((R_1 \parallel R_2) + R_B)]$$

$$g_m = \mu_n C_{\text{ox}}(Z/L)(V_{\text{GS}} - V_T) = \mu_n C_{\text{ox}}(Z/L)(V_G - V_T)$$

*(2 pts for correct  $g_m$  expression)*

Assume  $R_L$  is very large:

$$\therefore \text{gain} = -[\mu_n C_{\text{ox}}(Z/L)(V_G - V_T)] (R_C) [(R_1 \parallel R_2) / ((R_1 \parallel R_2) + R_B)]$$

*(2 pts for correct magnitude of the gain, but without the negative sign;*

*3 pts for correct gain)*

#### **PROBLEM FOUR(CONTINUED):**

B) Using the results from part A, assuming:

$$R_1=R_2=1 \text{ k}\Omega$$

$$R_B=R_C=100 \text{ }\Omega$$

$$\mu=1000 \text{ cm}^2/\text{V-sec}$$

$$L=1 \text{ }\mu\text{m}$$

$$C_p = 10^{-2} \text{ F/m}^2$$

Find the value of the transistor width  $Z$  that is required to give a voltage gain of 10 for this circuit.

$$\mu=1000 \text{ cm}^2/\text{V-sec} = 0.1 \text{ m}^2/\text{V-sec}$$

$$V_{\text{gs}} = [R_2 / (R_1 + R_2)] V_{\text{CC}} = 5\text{V}$$

$$|\text{gain}| = [\mu_n C_{\text{ox}}(Z/L)(V_G - V_T)] (R_C) [(R_1 \parallel R_2) / ((R_1 \parallel R_2) + R_B)]$$

$$10 = [0.1 \times 10^{-2} (Z/10^{-6})(5-V_T)](100)[(1 \text{ k}\Omega \parallel 1 \text{ k}\Omega) / ((1 \text{ k}\Omega \parallel 1 \text{ k}\Omega) + 100)]$$

$$10 = [10^3 Z (5-V_T)] (100) [500 / ((500 + 100)]$$

$$1.2 \times 10^{-4} = Z (5 - V_T)$$

$$\therefore Z = (1.2 \times 10^{-4}) / (5 - V_T)$$

*(Use the gain expression from part a):*

*3pts for finding  $V_{gs}$*

*8pts for finding  $V_{gs}$  and correct substitution, but wrong answer*

*10pts for correct answer*

*If no expression was found in part a), but show the steps for how to solve this question, 3 pts)*