# Quantized Conductance of Point Contacts in a Two-Dimensional Electron Gas

B. J. van Wees
*Department of Applied Physics, Delft University of Technology, 2628 CJ Delft, The Netherlands*

H. van Houten, C. W. J. Beenakker, and J. G. Williamson,
*Philips Research Laboratories, 5600 JA Eindhoven, The Netherlands*

L. P. Kouwenhoven and D. van der Marel
*Department of Applied Physics, Delft University of Technology, 2628 CJ Delft, The Netherlands*

and

C. T. Foxon
*Philips Research Laboratories, Redhill, Surrey RH1 5HA, United Kingdom*
(Received 31 December 1987)

Ballistic point contacts, defined in the two-dimensional electron gas of a GaAs-AlGaAs heterostructure, have been studied in zero magnetic field. The conductance changes in quantized steps of $e^2/\pi\hbar$ when the width, controlled by a gate on top of the heterojunction, is varied. Up to sixteen steps are observed when the point contact is widened from 0 to 360 nm. An explanation is proposed, which assumes quantized transverse momentum in the point-contact region.

PACS numbers: 72.20.Jv, 73.40.Cg, 73.40.Lq

As a result of the high mobility attainable in the two-dimensional electron gas (2DEG) in GaAs-AlGaAs heterostructures it is now becoming feasible to study ballistic transport in small devices.[1-6] In metals ideal tools for such studies are constrictions having a width $W$ and length $L$ much smaller than the mean free path $l_e$. These are known as Sharvin point contacts.[7] Because of the ballistic transport through these constrictions, the resistance is determined by the point-contact geometry only. Point contacts have been used extensively for the study of elastic and inelastic electron scattering. With use of biased point contacts, electrons can be injected into metals at energies above the Fermi level. This allows the study of the energy dependence of the scattering mechanisms.[8] With the use of a geometry containing two point contacts, with separation smaller than $l_e$, electrons injected by a point contact can be focused into the other contact, by the application of a magnetic field. This technique (transverse electron focusing) has been applied to the detailed study of Fermi surfaces.[9]

In this Letter we report the first experimental study of the resistance of ballistic point contacts in the 2DEG of high-mobility GaAs-AlGaAs heterostructures. The single-point contacts discussed in this paper are part of a double-point-contact device. The results of transverse electron focusing in these devices will be published elsewhere.[10] The point contacts are defined by electrostatic depletion of the 2DEG underneath a gate. This method, which has been used by several authors for the study of 1D conduction,[1,2] offers the possibility to control the width of the point contact by the gate voltage. Control of the width is not feasible in metal point contacts.

The classical expression for the conductance of a point contact in two dimensions (see below) is

$$G=(e^2/\pi\hbar)k_F W/\pi \quad (1)$$

in which $k_F$ is the Fermi wave vector and $W$ is the width of the contact. This expression is valid if $l_e \gg W$ and the Fermi wavelength $\lambda_F \ll W$. The first condition is satisfied in our devices, which have a maximum width $W_{max} \approx 250$ nm and $l_e = 8.5$ $\mu$m. The second condition should also hold when the devices have the maximum width. We expect quantum effects to become important when the width becomes comparable to $\lambda_F$, which is 42 nm in our devices. In this way we are able to study the transition from classical to quantum ballistic transport through the point contact.

The point contacts are made on high-mobility molecular-beam-epitaxy-grown GaAs-AlGaAs heterostructures. The electron density of the material is $3.56\times10^{15}/m^2$ and the mobility 85 $m^2/V$ s (at 0.6 K). These values are obtained from the devices containing the studied point contacts. A standard Hall bar geometry is defined by wet etching. Using electron-beam lithography, a metal gate is made on top of the heterostructure, with an opening 250 nm wide (inset in Fig. 1). The point contacts are defined by the application of a negative voltage to the gate. At $V_g = -0.6$ V the electron gas underneath the gate is depleted, the conduction taking place through the point contact only. At this voltage the point contacts have their maximum width $W_{max}$, about equal to the opening between the gates. By a further decrease of the gate voltage, the width of the point contacts can gradually be reduced, until they are fully

 © 1988 The American Physical Society

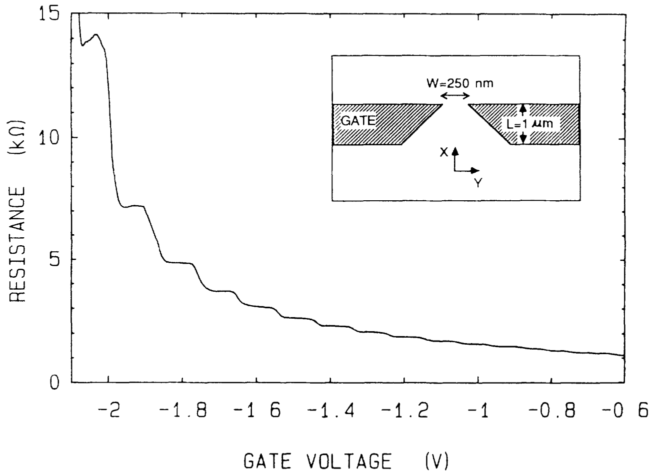



FIG. 1. Point-contact resistance as a function of gate voltage at 0.6 K. Inset: Point-contact layout.

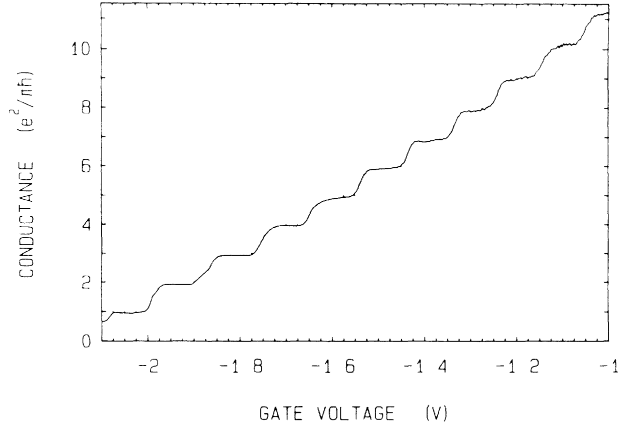



FIG. 2. Point-contact conductance as a function of gate voltage, obtained from the data of Fig. 1 after subtraction of the lead resistance. The conductance shows plateaus at multiples of $e^2/\pi\hbar$.

pinched off at $V_g = -2.2$ V.

We measured the resistance of several point contacts as a function of gate voltage. The measurements were performed in zero magnetic field, at 0.6 K. An ac lockin technique was used, with voltages across the sample kept below $kT/e$, to prevent electron heating. In Fig. 1 the measured resistance of a point contact as a function of gate voltage is shown. *Unexpectedly, plateaus are found in the resistance.* In total, sixteen plateaus are observed when the gate voltage is varied from $-0.6$ to $-2.2$ V. The measured resistance consists of the resistance of the point contact, which changes with gate voltage, and a constant series resistance from the 2DEG leads to the point contact. As demonstrated in Fig. 2, a plot of the conductance, calculated from the measured resistance after subtraction of a lead resistance of 400 Ω, shows clear plateaus at integer multiples of $e^2/\pi\hbar$. The above value for the lead resistance is consistent with an estimated value based on the lead geometry and the resistivity of the 2DEG. We do not know how accurate the quantization is. In this experiment the deviations from integer multiples of $e^2/\pi\hbar$ might be caused by the uncertainty in the resistance of the 2DEG leads. Inserting the point-contact resistance at $V_g = -0.6$ V (750 Ω) into Eq. (1) we find for the width $W_{\max} = 360$ nm, in reasonable agreement with the lithographically defined width between the gate electrodes.

The average conductance increases almost linearly with gate voltage. This indicates that the relation between the width and the gate voltage is also almost linear. From the maximum width $W_{\max}$ (360 nm) and the total number of observed steps (16) we estimate the increase in width between two consecutive steps to be 22 nm.

We propose an explanation of the observed quantization of the conductance, based on the assumption of quantized transverse momentum in the contact constriction. In principle this assumption requires a constriction much longer than wide, but presumably the quantization is conserved in the short and narrow constriction of the experiment. The point-contact conductance $G$ for ballistic transport is given by[7,11]

$$G = e^2 N_0 W(\hbar/2m)\langle |k_x|\rangle. \tag{2}$$

The brackets denote an average of the longitudinal wave vector $k_x$ over directions on the Fermi circle, $N_0 = m/\pi\hbar^2$ is the density of states in the two-dimensional electron gas, and $W$ is the width of the constriction. The Fermi-circle average is taken over discrete transverse wave vectors $k_y = \pm n\pi/W$ ($n = 1,2,\ldots$), so that we can write

$$\langle |k_x|\rangle = \frac{1}{2\pi k_\mathrm{F}} \int d^2k\, |k_x|\, \delta(k - k_\mathrm{F}) \frac{2\pi}{W} \sum_{n=1}^{\infty} \delta\left(k_y - \frac{n\pi}{W}\right). \tag{3}$$

Carrying out the integration and substituting into Eq. (2), one obtains the result

$$G = \sum_{n=1}^{N_c} \frac{e^2}{\pi\hbar}, \tag{4}$$

where the number of channels (or one-dimensional subbands) $N_c$ is the largest integer smaller than $k_\mathrm{F}W/\pi$. For

$k_F W \gg 1$ this expression reduces to the classical formula [Eq. (1)]. Equation (4) tells us that $G$ is quantized in units of $e^2/\pi\hbar$ in agreement with the experimental observation. With the increase of $W$ by an amount of $\lambda_F/2$, an extra channel is added to the conductance. This compares well with the increase in width between two consecutive steps, determined from the experiment. Equation (4) may also be viewed as a special case of the multichannel Landauer formula,[12-14]

$$G = \frac{e^2}{\pi\hbar} \sum_{n,m=1}^{N_c} |t_{nm}|^2, \tag{5}$$

for transmission coefficients $|t_{nm}|^2 = \delta_{nm}$ corresponding to ballistic transport with no channel mixing.

It is interesting to note that this multichannel Landauer formula has been developed to describe the idealized case of the resistance of a quantum wire, connected to massive reservoirs, in which the inelastic-scattering events are thought to take place exclusively. As discussed by Imry,[13] $|t_{nm}|^2 = \delta_{nm}$ corresponds to the case that elastic scattering is absent in the wire also. The fact that the conductance $G = N_c e^2/\pi\hbar$ of such an ideal wire is finite[15] is a consequence of the inevitable contact resistances associated with the connection to the thermalizing reservoirs. The findings described in this Letter may imply that we have realized an experimental system which closely approximates the behavior of idealized mesocopic systems.

In summary we have reported the first measurements of the conductance of single ballistic point contacts in a two-dimensional electron gas. A novel quantum effect is found: The conductance is quantized in units of $e^2/\pi\hbar$.

We would like to thank J. M. Lagemaat, C. E. Timmering, and L. W. Lander for technological support and L. J. Geerligs for assistance with the experiments. We thank the Delft Center for Submicron Technology for the facilities offered and the Stichting voor Fundamenteel Onderzoek der Materie (FOM) for financial support.

[1] T. J. Thornton, M. Pepper, H. Ahmed, D. Andrews, and G. J. Davies, Phys. Rev. Lett. **56**, 1198 (1986).

[2] H. Z. Zheng, H. P. Wei, D. C. Tsui, and G. Weimann, Phys. Rev. B **34**, 5635 (1986).

[3] K. K. Choi, D. C. Tsui, and S. C. Palmateer, Phys. Rev. B **32**, 5540 (1985).

[4] H. van Houten, C. W. J. Beenakker, B. J. van Wees, and J. E. Mooij, in Proceedings of the Seventh International Conference on the Physics of Two-Dimensional Systems, Santa Fe, 1987, Surf. Sci. (to be published).

[5] G. Timp, A. M. Chang, J. E. Cunningham, T. Y. Chang, P. Mankiewich, R. Behringer, and R. E. Howard, Phys. Rev. Lett. **58**, 2814 (1987).

[6] G. Timp, A. M. Chang, P. Mankiewich, R. Behringer, J. E. Cunningham, T. Y. Chang, and R. E. Howard, Phys. Rev. Lett. **59**, 732 (1987).

[7] Yu.V. Sharvin, Zh. Eksp. Teor. Fiz. **48**, 984 (1965) [Sov. Phys. JETP **21**, 655 (1965)].

[8] For a review, see I. K. Yanson and O. I. Shklyarevskii, Fiz. Nizk. Temp. **12**, 899 (1986) [Sov. J. Low Temp. Phys. **12**, 509 (1986)].

[9] P. C. van Son, H. van Kempen, and P. Wyder, Phys. Rev. Lett. **58**, 1567 (1987).

[10] H. van Houten, B. J. van Wees, J. E. Mooij, C. W. J. Beenakker, J. G. Williamson, and C. T. Foxon (to be published).

[11] I. B. Levinson, E. V. Sukhorukov, and A. V. Khaetskii, Pis'ma Zh. Eksp. Teor. Fiz. **45**, 384 (1987) [JETP Lett. **45**, 488 (1987)].

[12] R. Landauer, IBM J. Res. Dev. **1**, 223 (1957); R. Landauer, Phys. Lett. **85A**, 91 (1981).

[13] M. Buttiker, Y. Imry, R. Landauer, and S. Pinhas, Phys. Rev. B **31**, 6207 (1985). For a survey, see Y. Imry, in *Directions in Condensed Matter Physics,* edited by G. Grinstein and G. Mazenko (World Scientific, Singapore, 1986), Vol. 1, p. 102.

[14] D. S. Fisher and P. A. Lee, Phys. Rev. B **23**, 6851 (1981).

[15] The original Landauer formula (Ref. 12) containing the ratio of transmission and reflection coefficients does give an infinite conductance for a perfect system. However, this formula excludes contributions from the contact resistances.

# Controlled fabrication of metallic electrodes with atomic separation

A. F. Morpurgo and C. M. Marcus[a)]
*Department of Physics, Stanford University, Stanford, California 94305-4060*

D. B. Robinson
*Department of Chemistry, Stanford University, Stanford, California 94305-5080*

(Received 19 November 1998; accepted for publication 8 February 1999)

We report a technique for fabricating metallic electrodes on insulating substrates with separations on the 1 nm scale. The fabrication technique, which combines lithographic and electrochemical methods, provides atomic resolution without requiring sophisticated instrumentation. The process is simple, controllable, reversible, and robust, allowing rapid fabrication of electrode pairs with high yield. We expect the method to prove useful in interfacing molecular-scale structures to macroscopic probes and electronic devices. © *1999 American Institute of Physics.* [S0003-6951(99)04614-8]

Rapid advances in the ability to manipulate[1–3] and measure[4–7] matter at the level of single atoms and molecules suggest that future technology may allow the fabrication of electronic devices whose core consists of one or a few molecules. This possibility offers important technological advantages beyond a simple reduction in size, as single molecules can be designed and synthesized to perform a variety of specific electronic functions including molecular switches,[8] rectifiers,[9] magnetic and optically bistable systems,[10] and even molecular transistors,[11] allowing electronic functionality to be incorporated into chemical synthesis. However, what currently limits the systematic investigation of nanometer-scale electronic elements as well as their use as a viable technology (i.e., molecular electronics[12]) is the absence of a simple means of interfacing very small objects such as single molecules to macroscopic structures and devices.

At present, experiments probing the electrical properties of single atoms or molecules require either sophisticated techniques based on scanning probe microscopy, or special contacting schemes which often limit experimental flexibility. The latter is illustrated by the clever recent experiments measuring the electrical conductance of benzene–dithiol molecules using mechanical break junctions to provide two metallic contacts.[13] This approach works well but is not readily adapted to include electrostatic gates, a feature that would broaden the experimental possibilities. On the other hand, even the best conventional lithographic methods[14] cannot controllably produce electrodes separated by a few nanometers or less, which are necessary to contact most molecules of interest.

In this letter, we report a technique that readily allows the fabrication of pairs of metallic electrodes with atomic scale separation on an insulating substrate. The crucial innovation of this technique, which is based on standard lithography combined with electrochemical deposition, is active monitoring and control of the separation between electrodes *during the fabrication process*. The simplicity and robustness of the technique suggests that large-scale implementation for the purpose of nanoelectronic device fabrication should be possible.

The technique involves two main steps, as illustrated in Fig. 1. First, metallic electrodes are prepared using conventional microfabrication [Fig. 1(a)]. The separation between electrodes at this stage is not critical. In the second step, metal is electrodeposited on top of the existing pattern from an electrolyte solution [Fig. 1(b)]. This results in an increase in the size of the electrodes, and hence a decrease in their separation [Fig. 1(c)]. By measuring the electrical resistance between the two electrodes, we are able to monitor their separation once this distance becomes very small. In practice, monitoring the resistance signal allows controlled deposition with atomic-scale resolution. The process can be reversed to controllably widen gaps with similar accuracy. In fact, one can deposit until the electrodes are in contact and subsequently electrodissolve the metal to reopen the gap.

Examples of electrode pairs fabricated by this technique are shown in Fig. 2. Coarsely spaced Ti/Au (15 nm/35 nm) electrodes were patterned on a thermally oxidized silicon substate electron-beam lithography and liftoff. Initial spacings were in the range 50–400 nm. Samples were then placed in an aqueous solution consisting of 0.01 M potassium cyanaurate [$KAu(CN)_2$], and a buffer ($p$H 10) composed of 1 M potassium bicarbonate ($KHCO_3$) and 0.2 M potassium hydroxide. In the deposition reaction, the cyanau-

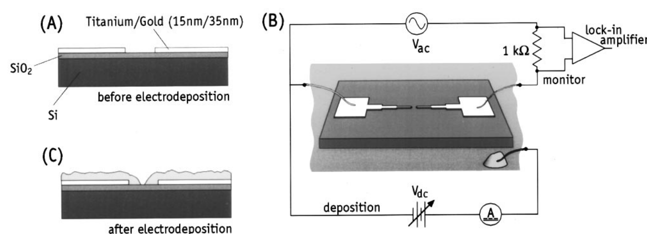



FIG. 1. Fabrication of nanoelectrodes consists of two main steps: (a) Electrodes with large separation are fabricated by conventional lithography. (b) Metal is electrodeposited onto the electrodes, reducing their separation. $V_{dc}$ controls electrodeposition while $V_{ac}$ is used to monitor the conductance and thus the separation between the electrodes. Reversing $V_{dc}$ allows material to be removed rather than deposited. (c) When deposition is stopped before the electrodes touch, separations on the 1 nm scale are obtained reproducibly.

[a)]Electronic mail: cmarcus@stanford.edu

 © 1999 American Institute of Physics
Downloaded 02 Apr 2004 to 128.200.240.127. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

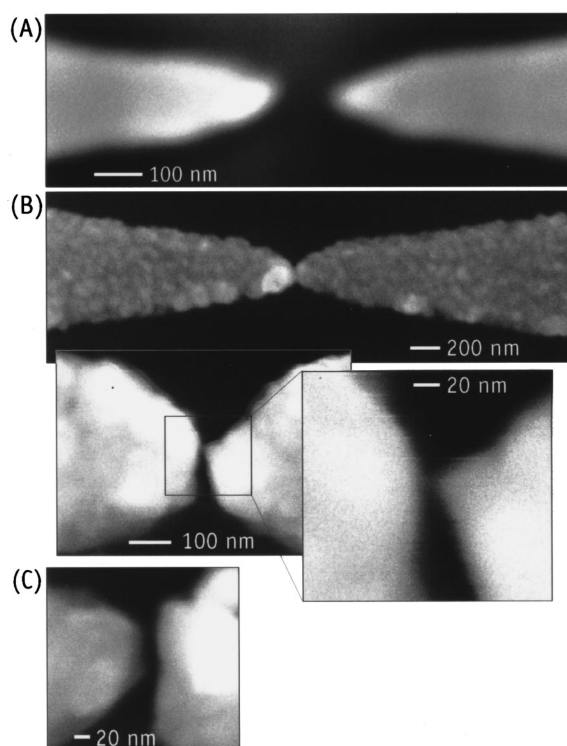



FIG. 2. SEM images before and after electrodeposition (scale bars show dimensions). (a) Electrodes before electrodeposition. (b) Electrodes after electrodeposition. The resolution of the SEM is 5 nm, not sufficient to resolve the gap. (c) Electrodes in which the gap was reopened by electrodissolution, by reversing $V_{dc}$ following an intentional short circuiting (contacting) in a previous electrodeposition process.

rate ion accepts an electron from the electrode and liberates the cyanide ligands, leaving a neutral gold atom at the surface. A gold pellet, 2–3 mm in diameter, was immersed in the solution to act as a counterelectrode. Thin gold wires (25 $\mu$m diam, with ~3–4 mm of length in contact with the solution) were used to connect the patterned electrodes and the counterelectrode to the electrical circuit shown in Fig. 1(b). The complete circuit simultaneously serves to drive the electrodeposition process as well as monitor the interelectrode resistance.

During electrodeposition, a voltage bias of −0.5 to −0.6 V was applied to both electrodes relative to the counterelectrode, inducing a deposition current of 2–3 $\mu$A, resulting in gold plating at a lateral rate of ~1 Å/s. A number of values for the deposition current were used successfully and no effort has been made yet to optimize the process. The resistance between the two electrodes was measured by applying a 4 mV alternating current (ac) bias at 1 Hz across the electrodes and measuring the ac ''monitor'' current through a 1 k$\Omega$ series resistor using a lock-in amplifier [Fig. 1(b)].[15]

Three phases of electrodeposition corresponding to different ranges of electrode separation can be identified from the time evolution of the monitor current. In the first phase, when the electrodes are far apart, the ac monitor current (~20 nA) is small and roughly constant [Fig. 3(a)]. This current is proportional to the immersed surface area of the electrodes (dominated by the surfaces of the 25 $\mu$m gold wires) and results from the ac modulation of the direct current (dc) deposition current. The second phase is marked by a sudden increase of the monitor current [Fig. 3(a), inset]. At this point the electrodes are already very close, less than 5 nm, as shown below. The additional current observed in this phase is presumably due to direct tunneling between the contacts, enhanced by the screening effect of ions in the gap, which reduces the height of the tunnel barrier.[16] The third phase, when the contacts finally touch, is marked by a sudden jump in the monitor current, followed by its saturation at a value given by the applied voltage divided by the ~1 k$\Omega$ series resistance.

During the second phase of electrodeposition, when the electrodes are very close together but not yet touching, the monitor current is extremely sensitive to electrode distance, enabling control of the separation on an atomic scale. This is illustrated by Fig. 3(c), in which the deposition rate was reduced by a factor of 50 (by reducing the deposition current to ~50 nA) following the increase in monitor current. Using such small deposition currents allows the first atom(s) connecting the two electrodes to be resolved. These first atoms bridging the gap between the electrodes give rise to jumps in the monitor current corresponding to steps of ~2 $e^2/h$ in the conductance [Fig. 3(c), left inset], as expected for a single gold atom,[7] which has a single electronic valence state available for conduction. Typically, only one or two steps of this magnitude are observed, followed by larger jumps presumably originating from clusters of atoms close to the contact point reassembling themselves into more energetically favorable configurations. These steps are similar to those seen in electrodeposited Cu nanowires made using a scanning tunneling microscope.[17]

The appearance of sharp steps in the monitor current associated with atomic conduction allows two important conclusions to be drawn. First, that this controlled deposition technique has atomic-scale resolution, so that it can be used to fabricate electrodes with ~1 nm separation reliably. Second, the steps unambiguously mark when the two electrodes touch; if electrodeposition is stopped at any earlier stage it is assured that the electrodes are not in direct contact.

We have fabricated many pairs of electrodes, stopping electrodeposition when the increase in the monitor current was first detected, and subsequently imaged the samples using a scanning electron microscope (SEM). Neither the SEM (Fig. 2) nor atomic force microscopy could resolve gap clearly, but placed consistent upper limits of 5 nm on the separation. Electrical resistances between such pairs of electrodes (measured using a 0.1 V bias in air after the fabrication) were between 1 and 30 G$\Omega$, and in a few cases as low as 0.5 G$\Omega$, whereas unplated electrodes on the same substrate had resistances above several hundred gigaohms, limited by the noise of the measurement. These values are consistent with electronic tunneling through a gap of roughly 1 nm.[18]

We emphasize that no tuning of fabrication parameters was needed to achieve the present results, demonstrating the robustness of the technique. Alternative strategies have been reported recently[19] capable of feature sizes approaching those reported here, however, the present method offers several advantages including extremely small gaps, high yield (approaching 100%) at gap sizes down to ~1 nm, relatively short fabrication time, and simple, readily available instrumentation.

Downloaded 02 Apr 2004 to 128.200.240.127. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

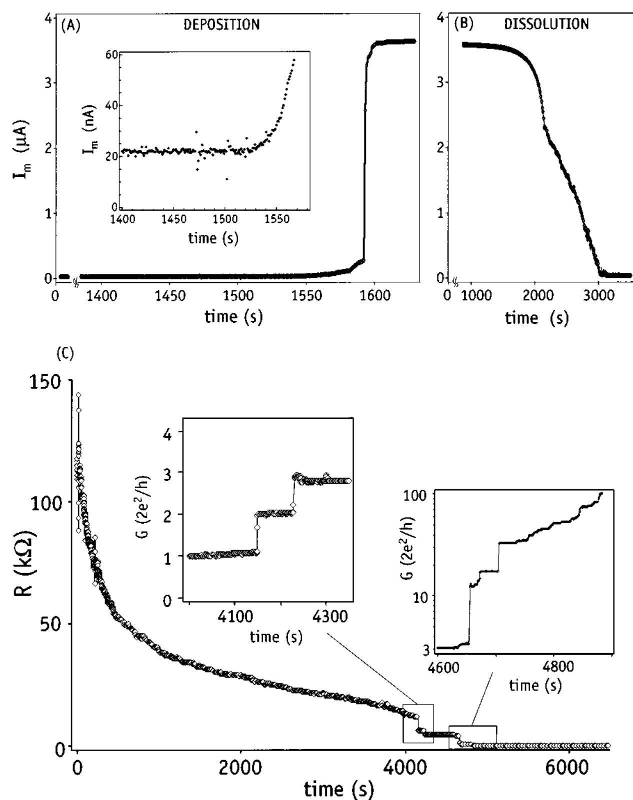



FIG. 3. Time evolution of the ac monitor current during (a) rapid electrodeposition and (b) electrodissolution. Three phases of electrodeposition can be identified. (1) In this example, for times before ~1540 s, a small ac monitor current is measured when the electrodes are well separated. (2) For times between ~1540 and 1590 s, a continuously increasing monitor current appears as the electrodes approach one another at the nanometer scale. (3) At ~1590 s, a sudden jump in the monitor current is observed as the electrodes make contact, followed by saturation. The time evolution is reversed for dissolution. (c) Time evolution of the resistance $R$ between electrodes for slow deposition [roughly 50 times slower than in (a)]. Conductance steps close to 2 $e^2/h$ (the expected value for Au atoms) are visible in the left inset. Following initial contact, plateau-like features and steps in the conductance on the order of a few $e^2/h$ persist as the contact between electrodes continues to increase in size at the atomic scale (right inset).

Because this process can employ techniques and instruments that are currently in use in a variety of industries, including microelectronics manufacturers (deep-ultraviolet lithography and electroplating), it may be readily realized in an industrial setting. Note also that electronic feedback can easily be incorporated into the monitoring scheme, allowing the electrodeposition rate to be adjusted as a function of the resistance between electrodes and then stopped at a specified separation. This type of feedback control lends itself to parallel operation and provides a means of fabricating many structures at the same time.

The authors thank C. E. D. Chidsey for useful discussions and for the use of equipment in his laboratory. Research supported by the National Science Foundation PECASE program, DMR-9629180-1, and the Stanford Center for Materials Research, NSF-MRSEC.

[1] D. M. Eigler and E. K. Scweizer, Nature (London) **344**, 524 (1990).
[2] M. F. Crommie, C. P. Lutz, and D. M. Eigler, Science **262**, 218 (1993).
[3] J. K. Gimzewski, C. Joachim, R. R. Schlittler, V. Langlais, H. Tang, and I. Johannsen, Science **281**, 531 (1998).
[4] F. F. Fan and A. J. Bard, Science **267**, 871 (1995).
[5] C. Joachim, J. K. Gimzewski, R. R. Schlittler, and C. Chavy, Phys. Rev. Lett. **74**, 2102 (1995).
[6] A. Yazdani, B. A. Jones, C. P. Lutz, M. F. Crommie, and D. M. Eigler, Science **275**, 1767 (1997).
[7] E. Scheer, N. Agrait, J. C. Cuevas, A. Levy Yeyati, B. Ludoph, A. Martin-Rodero, G. R. Bollinger, J. M. v. Ruitenbeek, and C. Urbina, Nature (London) **394**, 154 (1998).
[8] M. P. O'Neil, M. P. Niemczyk, W. A. Svec, D. Gosztola, G. L. Gaines III, and M. R. Wasielewski, Science **257**, 63 (1992).
[9] A. Aviram and M. A. Ratner, Chem. Phys. Lett. **29**, 277 (1974); M. Pomerantz, A. Aviram, R. A. McCorkle, L. Li, and A. G. Schrott, Science **255**, 1115 (1992).
[10] O. Kahn and C. J. Martinez, Science **279**, 44 (1998).
[11] C. Joachim and J. K. Gimzewski, Chem. Phys. Lett. **265**, 353 (1997); S. J. Tans, A. R. M. Verschuren, and C. Dekker, Nature (London) **393**, 49 (1998).
[12] For a very recent overview see J. Gimzewski, Phys. World **11**, 29 (1998).
[13] M. A. Reed, C. Zhou, C. J. Muller, T. P. Burgin, and J. M. Tour, Science **278**, 252 (1997).
[14] See for instance L. L. Sohn, C. T. Black, M. Eriksson, M. Crommie, and H. Hess, in *Mesoscopic Electron Transport*, Nato ASI Series, edited by L. L. Sohn, L. P. Kouwenhoven, and G. Schön (Kluwer, Dordrecht, 1997), and references therein.
[15] Similar *in situ* monitoring of the electrical properties of a device to control its fabrication has been used previously, see for instance E. S. Snow and P. M. Campbell, Science **270**, 1639 (1995); Y. Nakamura, D. L. Klein, and J. S. Tsai, Appl. Phys. Lett. **68**, 275 (1996); T. Schmidt, R. Martel, R. L. Sandstrom, and P. Avouris, *ibid.* **73**, 2173 (1998).
[16] See, e.g., W. Schmickler and D. Henderson, J. Electroanal. Chem. Interfacial Electrochem. **290**, 283 (1990).
[17] C. Z. Li and N. J. Tao, Appl. Phys. Lett. **72**, 894 (1998).
[18] Y. Kuk, in *Scanning Tunneling Microscopy*, edited by J. A. Stroscio and W. J. Kaiser (Academic, San Diego, 1993), p. 281.
[19] D. L. Klein, P. L. McEuen, J. E. Bowen Katari, R. Roth, and A. P. Alivisatos, Appl. Phys. Lett. **68**, 2574 (1996); A. Bezryadin and C. Dekker, J. Vac. Sci. Technol. B **15**, 793 (1997); A. Bezryadin, C. Dekker, and G. Schmid, Appl. Phys. Lett. **71**, 1273 (1997).

Downloaded 02 Apr 2004 to 128.200.240.127. Redistribution subject to AIP license or copyright, see http://apl.aip.org/apl/copyright.jsp

# Microfabrication of a mechanically controllable break junction in silicon

C. Zhou, C. J. Muller, M. R. Deshpande, J. W. Sleight, and M. A. Reed
*Center for Microelectronic Materials and Structures, Yale University, P.O. Box 208284, New Haven, Connecticut 06520-8284*

(Received 6 April 1995; accepted for publication 20 June 1995)

We present a detailed description of the fabrication and operation at room temperature of a novel type of tunnel displacement transducer. Instead of a feedback system it relies on a large reduction factor assuring an inherently stable device. Stability measurements in the tunnel regime infer an electrode stability within 3 pm in a 1 kHz bandwidth. In the contact regime the conductance takes on a discrete number of values when the constriction is reduced atom by atom. This reflects the conduction through discrete channels. © *1995 American Institute of Physics.*

Micromachining in silicon is an ongoing effort to provide ever smaller devices used as the active part of a sensor. Currently, it is straightforward to produce suspended beams, small springs, and vibrating or rotating structures on a chip. Engineers can make use of a number of classical transducer phenomena, such as piezoelectricity, piezoresistivity and capacitance changes to convert displacements into an electrical signal. However, the formation of smaller sensors is often obtained at the cost of precision, since the signal of the above mentioned transducer phenomena scale with size. In contrast to classical transducers, a tunnel transducer[1] (e.g., an STM) is compatible with further miniaturization and possesses an astonishing sensitivity to displacements. When a vacuum tunnel gap between two metallic electrodes is increased by 1 Å, the tunnel resistance increases approximately by an order of magnitude. This has been realized by a number of groups who have used tunnel sensors in devices.[2] The extreme sensitivity of these sensors on positional displacements however implies that the practical range of operation is limited to distances smaller than 5 Å since at larger distances the resistance becomes almost infinite and unmeasurable.

In conventional STM embodiments, one electrode is usually mounted on a flexible lever, which can be moved by an electrical signal. The tunnel gap is kept constant with the use of a feedback system, necessary since temperature fluctuations, (acoustic) vibrations or other disturbances will otherwise change the vacuum gap over distances much larger than the practical range. An accelerometer, magnetometer, and an infrared sensor have been successfully developed with these kind of tunnel sensors in feedback operation.[2] Despite these successes we have used a different approach and constructed an inherently stable tunnel sensor. When used as a displacement sensor this device can be fabricated in such a way that the electrode separation during operation remains in the practical range of about 5 Å. Due to the extreme stability of this device it can be operated without feedback; however it may also be used in a feedback loop. In this letter we present the fabrication and operation of this new type of tunnel sensor which was proposed in Ref. 3. It is inherently stable, adjustable, and compatible with silicon technology. Detailed measurements are shown, in both the contact and tunnel regimes.

The principle of operation and a schematic perspective and cross sectional view of the device are shown in Fig. 1. The starting material is a ⟨100⟩ oriented 250 $\mu$m thick silicon wafer with an oxide layer of 400 nm. Standard electron-beam lithography is used to define a pattern in a PMMA bilayer used for the evaporation of an adhesion layer (10 Å Ti) and 800 Å of gold onto the oxide. The gold film has a shape as indicated in Fig. 1(a). Next a photolithographically defined thick layer of aluminum is evaporated everywhere on the oxide except over a distance $u$, centered around the smallest gold feature. The next step uses the gold and alumi-

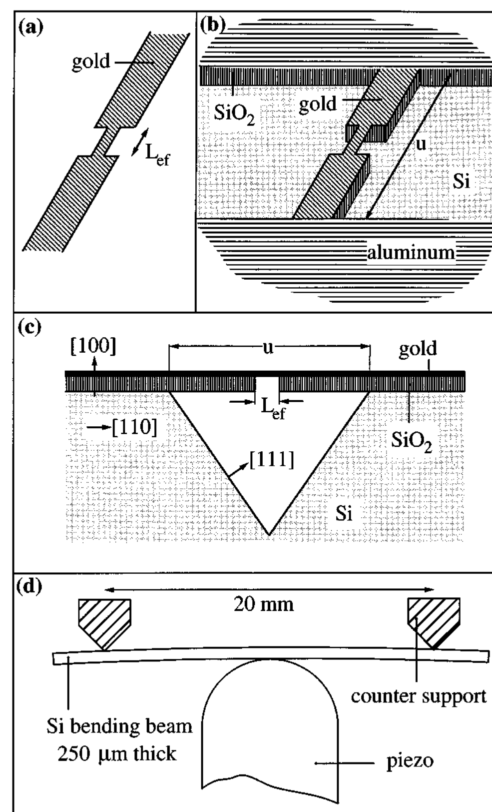



FIG. 1. (a) The gold wire defined by electron-beam lithography. The smallest width of the wire is 100 nm, $L_{eff}$ is about 250 nm. (b) Both the aluminum and gold film are used as an etch mask to etch through the $SiO_2$ into the Si. (c) A cross section along the gold wire after the pit is etched into the silicon. Si etching is stopped at the concave corners and the intersection between the ⟨111⟩ crystallographic surface and the $SiO_2$ edges. (d) The mounting configuration of the silicon bending beam in a break junction setup.

 0003-6951/95/67(8)/1160/3/$6.00 © 1995 American Institute of Physics

Downloaded¬02¬Apr¬2004¬to¬128.200.240.127.¬Redistribution¬subject¬to¬AIP¬license¬or¬copyright,¬see¬http://apl.aip.org/apl/copyright.jsp

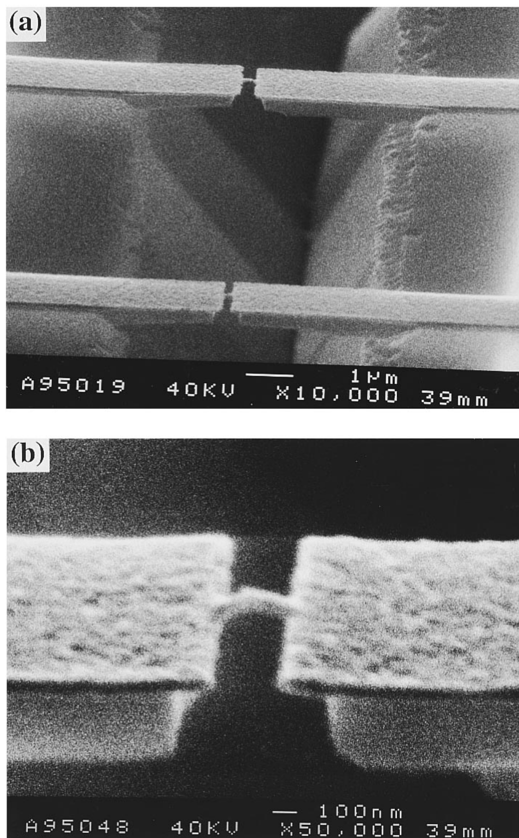



FIG. 2. (a) Two devices suspended above a triangular pit in the Si substrate before the connecting wire is broken in the break junction setup. Each device shows two $SiO_2$ cantilevers which are covered and bridged by the gold wire. (b) A close-up showing the connecting wire. Before operating the device in the contact or tunnel regime the small connecting wire has to be broken. Some undercut of the gold is present due to the imperfection of the reactive ion etching process.

num films as a mask to etch through the $SiO_2$ into the Si with a $CF_4/O_2$ plasma [Fig. 1(b)]. The aluminum is then removed using a standard wet etch. The last step is a wet etch of the exposed Si area using a pyrocatechol-ethylene-diamine mixture.[4] Since the two cantilevers are aligned with the $\langle 110 \rangle$ direction in the substrate, a triangular pit is etched into the silicon, bounded by the $SiO_2$ edges and the $\langle 111 \rangle$ surfaces. Rapid undercutting at the convex corners by this etchant assures that the two cantilevers are free standing after the etching process.[5] The final device consists of two small cantilever beams ($2.5 \mu$m long, 4 $\mu$m wide) connected with a 100 nm wide wire over a length $L_{\mathrm{eff}}$ [Fig. 1(c)].

The device is mounted against two counter supports, approximately 20 mm apart, in a break junction configuration.[3] A force is exerted on the backside via the piezo element which is moved towards the device using a course adjustment screw [Fig. 1(d)]. The silicon beam is strained, resulting in an elongation of the top layer. The elongation of $u$ is concentrated on $L_{\mathrm{eff}}$, resulting in the fracture of the gold wire while the Si substrate stays intact (even though gold is more ductile than silicon). The piezo element has a maximum elongation of 5 $\mu$m and is used for fine adjustment of either atomic size contacts or vacuum barrier tunnel junctions between the fractured gold electrodes. Figure 2 shows a

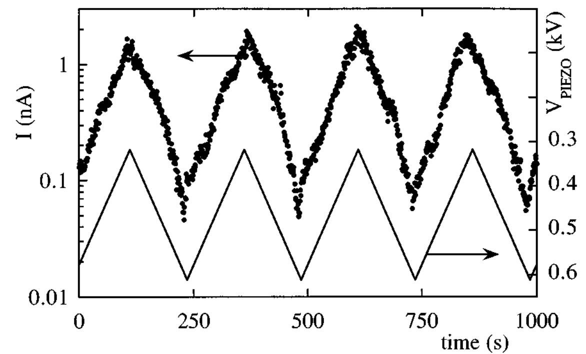



FIG. 3. The piezo voltage is changed in a triangular way (lower curve). The almost linear behavior of the tunnel current on a logarithmic scale reflects the exponential dependence on electrode separation. Note the large time scale, indicating the long term stability of the junction.

SEM photograph of a device before the bridging wire is broken. A 100 nm wire bridging the two cantilevers can be seen, and a slight undercut of the gold is visible. The etched pit into the Si [Fig. 2(a)] is bounded by a relatively rough $SiO_2$ edge, caused by the photolithography step. Some of the undercut below the $SiO_2$ layer results from this roughness and enlarges $u$ to about 10 $\mu$m.

Experiments are performed at room temperature in a vacuum system ($10^{-7}$Torr) which uses an oil-free absorption/ion-pump combination in order to reduce contamination of the exposed electrodes with hydrocarbons. Figure 3 illustrates the long term stability and the exponential dependence of the tunnel current $I_t$ on the vacuum barrier gap distance of this device. The junction is biased at 100 mV while a triangular voltage wave is applied to the piezo element (lower curve in Fig. 3). The variation in the piezo length induces a variation in the gap distance resulting in a change of the tunnel resistance (top curve in Fig. 3). The exponential dependence of $I_t$ on the gap distance $s$ is given by $I_t \propto \exp - \alpha \sqrt{\Phi} s$ with $\alpha = 1.025 \text{Å}^{-1} \text{eV}^{-1/2}$ and $\Phi$ is the work function of the gold electrodes. As the electrodes are displaced over about 2 Å the tunnel current changes over almost two orders of magnitude. The reason for this exceptional stability is the smallness of $u$ which determines the reduction factor $r$ (the ratio between the piezo elongation and the induced electrode separation). For our devices we estimate $r \simeq 5 \times 10^4$.[3] From two devices we experimentally infer, from the known piezo elongation and assuming an exponential dependence of the tunnel current with $\Phi = 4$ eV, $r \simeq 10^4$. The discrepancy of a factor of five may be due to nonuniform strain near the etched pit. In the tunnel regime the current noise amplitude, which depends on the tunnel resistance, is determined at a 100 mV bias for tunnel resistances between 100 k$\Omega$ and 10 M$\Omega$ in a 1 kHz bandwidth. In this resistance range the experimental value for the current noise amplitude implies about 3 pm fluctuations in the tunnel gap distance. Although we do not know the exact origin of these fluctuations, a detailed noise analysis should include the thermal agitation of the cantilever.[6]

When the electrodes are brought close enough together, a contact is formed. Experiments performed in the contact regime are done in the following way: the contact is reduced



Downloaded¬02¬Apr¬2004¬to¬128.200.240.127.¬Redistribution¬subject¬to¬AIP¬license¬or¬copyright,¬see¬http://apl.aip.org/apl/copyright.jsp

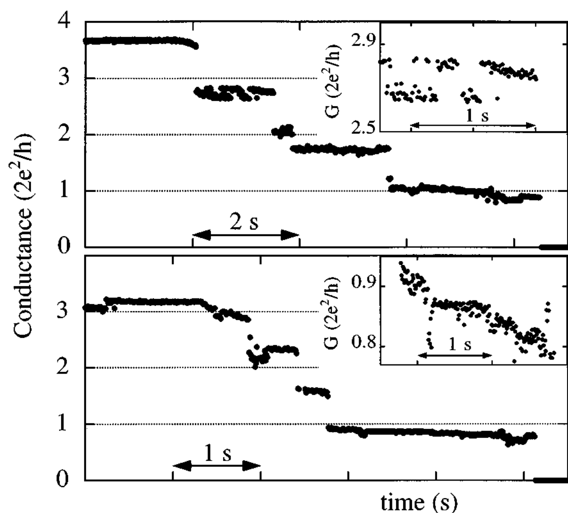



FIG. 4. Two conductance traces recorded when an atomic scale contact reduces its cross section as a function of time. Conductance plateaus are found to be near integer multiples of $2e^2/h$, reflecting the conduction through single channels. The insets show two types of intrinsic noise present in the contact regime.

in size by increasing the piezo voltage until the conductance of the contact is approximately 10 times $2e^2/h$. Then the piezo voltage is fixed, and it is found that the contact relaxes by itself, until eventually a jump to the tunnel regime takes place. Before this jump occurs, the two electrodes may be bridged by a single atom. We tentatively attribute this effect to outdiffusion of atoms, thus decreasing the constriction size. The junction is biased at 26 mV and the current is measured with a sample rate of 100 Hz. Typically the conductance decreases discontinuously as a function of time. Many conductance traces show plateaus near integer multiples of $2e^2/h$, and often the last plateau in the contact regime is near $2e^2/h$ (Fig. 4). After this smallest possible contact, the jump to the tunnel regime results in almost zero conductance (vacuum tunneling only). Upon close inspection, it is seen that the majority of the plateaus are not at exact integers. Backscattering in these metallic point contacts may be responsible for these observations.[7] The description in terms of conductance channels is still valid, although with transmission coefficients slightly different from one or zero.

Conductance noise is clearly present on the plateaus in Fig. 4. This noise is not due to external disturbances and its amplitude is much larger than the measurement accuracy. In general, two different types of noise can be present. The switching of one or a few atoms between energetically equifavorable positions in the contact region can result in closely spaced conductance levels (inset in upper panel of Fig. 4). The high kinetic energy of the atoms at room temperature can drive them between various sites, thus influencing the conductance. Another type of noise has a more random nature (inset in lower panel of Fig. 4). This may be due to small strain variations and small out-of-equilibrium displacements (small compared to the lattice constant) of a group of atoms comprising the contact.

In conclusion, we have presented a new type of displacement transducer, which is inherently stable. We have shown the operation of this device with gold electrodes as well in the contact as in the tunnel regime. The device was shown to be sensitive to positional changes of a single atom.

We would like to thank B.J. Vleeming for his assistance in building the high vacuum system. We acknowledge D.E. Prober and T.N. Todorov for stimulating discussions and the latter for providing us with Ref. 7 prior to publication. C.J.M. gratefully acknowledges the Niels Stensen Foundation for financial support. We acknowledge ARPA for financial support.

[1] M. F. Bocko, K. A. Stephenson, and R. H. Koch, Phys. Rev. Lett. **61**, 726 (1988).
[2] T. W. Kenny, S. B. Waltman, J. K. Reynolds, and W. J. Kaiser, Appl. Phys. Lett. **58**, 100 (1991); H. K. Rockstad, T. W. Kenny, J. K. Reynolds, W. J. Kaiser, and Th. B. Gabrielson, Sens. Actuators A **43**, 107 (1994), and references therein.
[3] C. J. Muller and R. de Bruyn Ouboter, J. Appl. Phys. **77**, 5231 (1995).
[4] G. Kaminsky, J. Vac. Sci. Technol. B **3**, 1015 (1985).
[5] K. E. Petersen, IEEE Trans. Electron Devices **ED-25**, 124 (1978).
[6] The resonance frequency of the cantilever is about 70 MHz. At room temperature it may be driven by $k_BT$ resulting in a deflection of about 1.5 pm; see Th. G. Gabrielson, IEEE Trans. Electron Devices **ED-40**, 903 (1993).
[7] A. M. Bratkovsky, A. P. Sutton, and T. N. Todorov, Phys. Rev. B (to be published).



Downloaded¬02¬Apr¬2004¬to¬128.200.240.127.¬Redistribution¬subject¬to¬AIP¬license¬or¬copyright,¬see¬http://apl.aip.org/apl/copyright.jsp

# Single-Walled Carbon Nanotube Electronics

Paul L. McEuen, Michael S. Fuhrer, and Hongkun Park

***Abstract*—Single-walled carbon nanotubes (SWNTs) have emerged as a very promising new class of electronic materials. The fabrication and electronic properties of devices based on individual SWNTs are reviewed. Both metallic and semiconducting SWNTs are found to possess electrical characteristics that compare favorably to the best electronic materials available. Manufacturability issues, however, remain a major challenge.**

***Index Terms*—Field-effect transistors (FETs), interconnections, nanotechnology, nanotube.**

## I. Introduction

SINGLE-WALLED carbon nanotubes (SWNTs) are nanometer-diameter cylinders consisting of a single graphene sheet wrapped up to form a tube. Since their discovery in the early 1990s [1] and [2], there has been intense activity exploring the electrical properties of these systems and their potential applications in electronics. Experiments and theory have shown that these tubes can be either metals or semiconductors, and their electrical properties can rival, or even exceed, the best metals or semiconductors known. Particularly illuminating have been electrical studies of individual nanotubes and nanotube ropes (small bundles of individual nantoubes). The first studies on metallic tubes were done in 1997 [3] and [4] and the first on semiconducting tubes in 1998 [5]. In the intervening five years, a large number of groups have constructed and measured nanotube devices, and most major universities and industrial laboratories now have at least one group studying their properties. These electrical properties are the subject of this review. The data presented here are taken entirely from work performed by the authors (in collaboration with other researchers), but they can be viewed as representative of the field.

The remarkable electrical properties of SWNTs stem from the unusual electronic structure of the two-dimensional material, graphene, from which they are constructed [6] and [7]. Graphene—a single atomic layer of graphite—consists of a 2-D honeycomb structure of $sp^2$ bonded carbon atoms, as seen in Fig. 1(a). Its band structure is quite unusual; it has conducting states at $E_f$, but only at specific points along certain directions in momentum space at the corners of the first Brillouin zone, as is seen in Fig. 1(b). It is called a zero-bandgap semiconductor since it is metallic in some directions and semiconducting in the others. In an SWNT, the momentum of the electrons moving around the circumference of the tube is quantized, reducing the available states to slices through the 2-D band structure, is illustrated in the Fig. 1(b). This quantization results in tubes that are either one-dimensional metals or semiconductors, depending on how the allowed momentum states compare to the preferred directions for conduction. Choosing the tube axis to point in one of the metallic directions results in a tube whose dispersion is a slice through the center of a cone [Fig. 1(c)]. The tube acts as a 1-D metal with a Fermi velocity $v_f = 8 \times 10^5$ m/s comparable to typical metals. If the axis is chosen differently, the allowed $k$s take a different conic section, such as the one shown in Fig. 1(d). The result is a 1-D semiconducting band structure, with a gap between the filled hole states and the empty electron states. The bandgap is predicted to be $E_g = 0.9$ eV/d[nm], where $d$ is the diameter of the tube. Nanotubes can, therefor,e be either metals or semiconductors, depending on how the tube is rolled up. This remarkable theoretical prediction has been verified using a number of measurement techniques. Perhaps the most direct used scanning tunneling microscopy to image the atomic structure of a tube and then to probe its electronic structure [8] and [9].

To understand the conducting properties of nanotubes, it is useful to employ the two-terminal Landauer–Buttiker Formula, which states that, for a system with $N$ 1-D channels in parallel: $G = (Ne^2/h)T$, where $T$ is the transmission coefficient for electrons through the sample (see, for example, [10]). For a SWNT at low doping levels such that only one transverse subband is occupied, $N = 4$. Each channel is fourfold degenerate, due to spin degeneracy and the sublattice degeneracy of electrons in graphene. The conductance of a ballistic SWNT with perfect contacts ($T = 1$) is then $4e^2/h = 155$ $\mu$S, or about 6.5 k$\Omega$. This is the fundamental contact resistance associated with 1-D systems that cannot be avoided. Imperfect contacts will give rise to an additional contact resistance $R_c$. Finally, the presence of scatters that give a mean-free path $l$ contribute an Drude-like resistance to the tube, $R_t = (h/4e^2)(L/1)$, where $L$ is the tube length. The total resistance is approximately the sum of these three contributions, $R = h/4e^2 + R_c + R_t$. In the sections below, we will analyze the conducting properties of metal and semiconducting nanotubes to infer the contact resistances, mean-free paths, conductivities, etc. We will concentrate almost exclusively on room temperature behavior. At low temperatures, SWNT devices exhibit a number of interesting quantum phenomena, including single-electron charging, quantum interference, Luttinger liquid behavior, and the Kondo

Manuscript received February 12, 2002; revised February 26, 2002. The work of P. L. McEuen was supported in part by the National Science Foundation (NSF) Center for Nanoscale Systems and the Microelectronics Advanced Research Corporation (MARCO) Focused Center Research Program (FCRP) on Materials, Structures, and Devices which is funded at the Massachusetts Institute of Technology, in part by MARCO under Contract 2001-MT-887 and by the Defense Advanced Research Projects Agency (DARPA) under Grant MDA972-01-1-0035.

P. L. McEuen is with the Laboratory of Atomic and Solid State Physics, Cornell University, Ithaca, NY 14853 USA.

M. S. Fuhrer is with the Department of Physics, University of Maryland, College Park, MD 20742 USA.

H. Park is with the Department of Chemistry and Chemical Biology, Harvard University, Cambridge, MA 02138 USA.

Publisher Item Identifier S 1536-125X(02)04581-7.

1536-125X/02$17.00 © 2002 IEEE

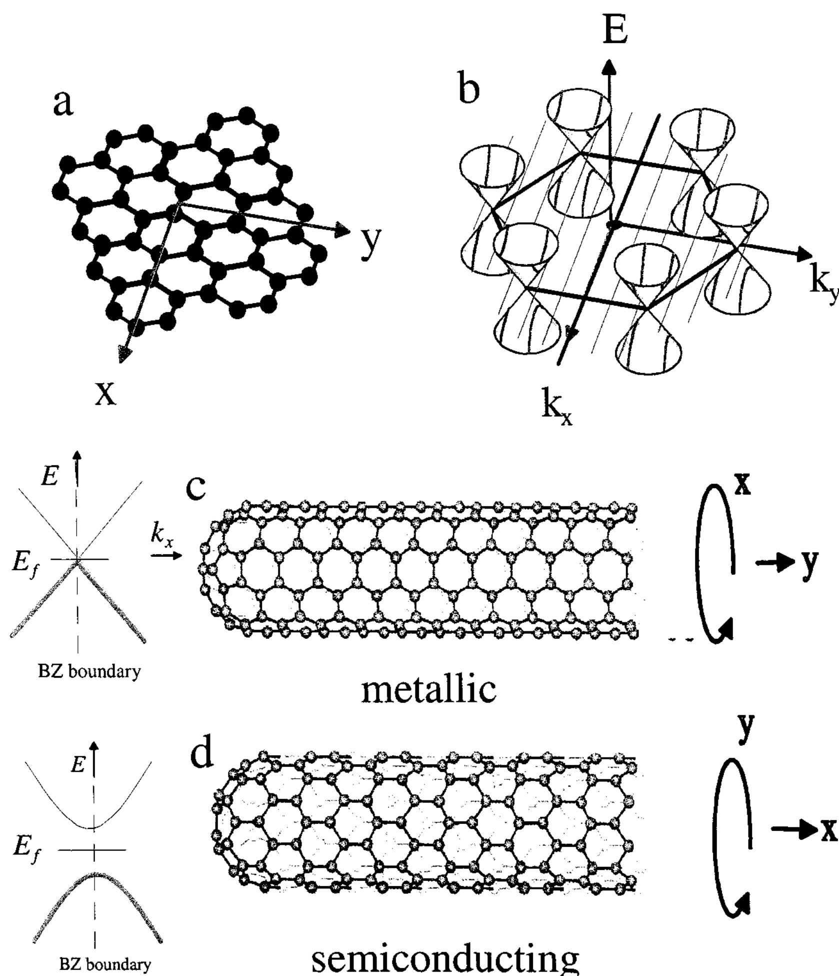



Fig. 1. (a) Lattice structure of graphene, a honeycomb lattice of carbon atoms. (b) Energy of the conducting states as a function of the electron wavevector $k$. There are no conducting states except along special directions where cones of states exist. (c), (d) Graphene sheets rolled into tubes. This quantizes the allowed $k$s around the circumferential direction, resulting in 1-D slices through the 2-D band structure in (b). Depending on the way the tube is rolled up, the result can be either (c) a metal or (d) a semiconductor.

effect, but these are not of direct relevance to most device applications. We, therefore, refer the reader to existing reviews for further discussion of these topics [11]–[13].

The critical issues with respect to device applications are twofold. The first is how reproducibly and reliably nanotube devices can be manufactured. Some current approaches to device fabrication are discussed in Section II. The second issue is how the electrical properties of SWNT devices compare to other electronic materials. These properties are described below in Sections III and IV for metallic and semiconducting tubes, respectively. These sections show that devices based on individual SWNTs have remarkable electrical characteristics, making them a very promising new class of electronic materials. The manufacturability challenges, however, are very significant. While advances are being made, controlled, reproducible device fabrication remains an unattained goal. These issues will be discussed in more detail in Section V.

## II. Nanotube Growth and Device Fabrication

SWNTs are grown by combining a source of carbon with a catalytic nanostructured material such as iron or cobalt at elevated temperatures. Sources of carbon employed to date include bulk graphite, hydrocarbons, and carbon monoxide. While the details of the growth process are far from understood, the basic elements are now coming into focus. A schematic is shown in Fig. 2(a). At elevated temperatures, the catalyst has a high solubility for carbon. The carbon in the particle links up to form graphene and wraps around the catalyst to from a cylinder. Subsequent growth occurs from the continuous addition of carbon to the base of the tube at the nanoparticle/tube interface. Remarkably, tubes can grow to lengths of hundreds of microns by this process [14].

Creating the proper conditions for growth can done in a variety of ways. From the point of view of device fabrication, the techniques can be divided into categories. In the first category are tubes grown by bulk synthesis techniques that are subsequently deposited on a substrate to make devices ("deposited tubes"). The most common methods for bulk fabrication are arc synthesis [1], [2] and laser assisted growth [15], and commercial sources of SWNTs from these techniques are now available. By controlling the growth conditions, high yields of SWNTs with narrow size distributions can be obtained. Unfortunately, tubes fabricated this way are in the form of a highly tangled "felt" of tubes and bundles of tubes. For electronic devices, these tubes

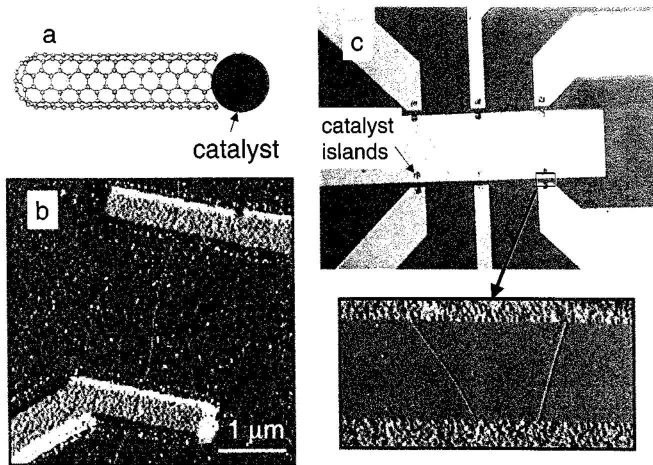



Fig. 2. (a) Schematic of a SWNT growing from a catalyst seed particle. (b) Atomic force microscope images of a single nanotube device fabricated using electron beam lithography. (c) Parallel fabrication of SWNT devices by growth from patterned catalysts and subsequent deposition of arrays of electrodes. The lower panel shows an AFM image of one pair electrodes bridged by two SWNTs.

must be separated, cut into usable sizes, and then deposited on a substrate. This is typically done by ultrasonication in an appropriate solvent to disperse and cut the SWNTs, followed by deposition onto a substrate by spinning or drying. Unfortunately, this is to date an uncontrolled process, producing tubes on the substrate of varying lengths that are often still bundled together. This processing can also induce significant numbers of defects in the tubes. However, new techniques for the wet processing, cutting, and sorting of nanotubes are under constant development [16]–[20].

An alternative approach is to grow the nanotubes directly on the wafer [21]. Currently this is done using chemical vapor deposition (CVD). The catalyst material is placed on the surface of a wafer, which is inserted in a standard furnace at 700 °C–1000 °C in a flow of a carbon source gas such as methane. The tubes grow from the catalyst seeds on the substrate. Engineering the properties of the catalyst and controlling the growth conditions control the properties of the tubes. For example, relatively monodisperse nanoparticle catalysts have been shown to yield SWNTs with a diameter closely matching that of the catalyst particle [22] and [23].

For both deposited and CVD-grown SWNTs, the tubes must be integrated with electrodes and gates on a wafer to make devices. A major challenge is the placement of the tubes relative to lithographically patterned features on the substrate. For both CVD-grown and deposited tubes, techniques have been developed that are satisfactory for research purposes, if not for mass production. Examples are shown in Fig. 2. For the device in Fig. 2(b), SWNTs were grown by CVD and located relative to alignment marks on the surface using an atomic force microscope. Polymethylmethacrylate (PMMA) resist was then spun over the tubes and an electron beam mask was designed, followed by electron beam lithography and liftoff to attach the gold leads [4]. The tubes remain bound to the substrate are unaffected by standard solvents for resist patterning. An alternate approach [21] is to pattern arrays of small catalyst islands from which SWNTs are grown. Electrode arrays are then deposited over the catalyst pads using optical or electron beam lithography. The result is pairs of electrodes with a random number of tubes connecting them, as seen in Fig. 2(c). By adjusting the parameters, a significant fraction of electrodes with only one tube bridging them can be obtained. Equivalent approaches exist to create devices for deposited tubes, with the CVD growth step replaced by a deposition step. An alternative method available for deposited tubes is to pattern the electrodes first and then deposit the tubes on top of the electrodes [3]. This avoids the high-temperature growth step, and chemical modification of the surface [24] and/or electric fields can be used to control, to some degree, the locations of the deposited tubes.

A schematic of the resulting device geometry is shown in the inset to Fig. 5. Source and drain electrodes allow the conducting properties of the nanotube to be measured, and a third gate electrode gate is used to control the carrier density on the tube. Typically, the degenerately doped Si substrate is used as the gate. Nearby metal electrodes [3], an oxidized Al electrode under the tube [25], and even an ionic solution around the tube [26] and [27] have also been employed as gates. When the conductance of the tube as the gate voltage, and hence the charge per unit length of the tube, is varied is measured, two classes of behavior are seen. For some tubes, $G$ is relatively independent of $V_g$, corresponding to a metallic tube. These are discussed in Section III. For other tubes, a dramatic dependence of $G$ on $V_g$ is seen, indicating semiconducting tubes. These will be discussed in Section IV.

## III. Electrical Properties of Metallic Tubes

Devices made from metallic SWNTs were first measured in 1997 [3] and [4], and have been extensively studied since that time. Two-terminal conductances of metallic SWNTs at room temperature can vary significantly, ranging from as small as $\sim$6-k$\Omega$ to several megaohms (M$\Omega$). Most of this variation is due to variations in contact resistance between the electrodes and the tube. As techniques for making improved contacts have been developed, the conductances have steadily improved. The best contacts have been obtained by evaporating Au or Pt over the tube, often followed by a subsequent anneal. A number of groups have seen conductances approaching the value, $G = 4e^2/h$, predicted for a *ballistic* nanotube [28] and [29]. An example is shown in Fig. 3, where the $dI/dV$ as a function of $V_{sd}$ is shown for a $\sim$1-$\mu$m long SWNT. At low $V_{sd}$, the conductance is $\sim 2\,e^2/h$, growing to $\sim 3.4e^2/h$ at the temperature is lowered. Assuming perfect contacts, this indicates that the mean-free path is at least $\sim 1$ $\mu$m at room temperature and grows even larger as the device is cooled. A number of other measurements corroborate this conclusion, such as measurements of short tubes where $G = 4e^2/h$ is found [28] and [29], and scanned probe experiments that probe the local voltage drop along the length of the nanotube [30]. This mean-free path corresponds to a room temperature resistivity of $\rho \sim 10^{-6}$ cm. The conductivity of metallic nanotubes can, thus, be equal to, or even exceed, the conductivity of the best metals at room temperature.

These long scattering lengths are in striking contrast to the behavior observed in traditional metals like copper, where scattering lengths are typically on the order of tens of nanometers

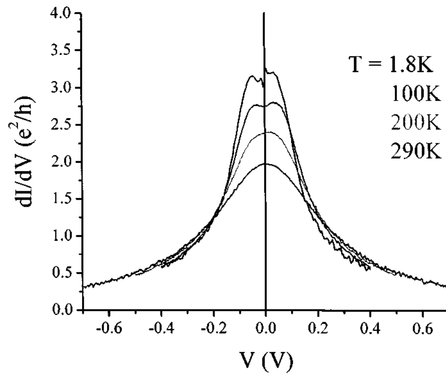



Fig. 3. Differential conductance $dI/dV$ of a metallic SWNT as a function of $V_{sd}$, at different temperatures. The conductance at low $V_{sd}$ approaches the values for a ballistic SWNT, $4e2/h$. At higher $V_{sd}$, the conductance drops dramatically due to optic and zone-boundary phonon scattering.

at room temperature, due to phonon scattering. The main difference is the significantly reduced phase space for scattering by acoustic phonons in a 1-D system. At room temperature, acoustic phonons have much less momentum than the electrons at the Fermi energy. In a traditional metal, phonons backscatter electrons through a series of small angle scattering events that eventually reverse the direction of an electron. This is not possible in a 1-D conductor such as a nanotube, where only forward and backward propagation is possible. Note that while the mean-free path is much larger than traditional metals, the conductivity is only comparable to slightly better. This is because the effective density of states in nanotubes is much lower than traditional metals because of the semimetallic nature of graphene.

Optic and zone-boundary phonons have the necessary momentum to backscatter electrons in nanotubes. They are too high in energy ($hf \sim 150$ meV) to be present at room temperature and low $V_{sd}$. At high source–drain voltages, however, electrons can emit these phonons and efficiently backscatter. This leads to a dramatic reduction of the conductance at high biases, as was first reported by Yao *et al.* [31]. This can be readily seen in the data of Fig. 3. The scattering rate grows linearly with $V_{sd}$, leading to a saturation of the total current through the tube. This saturation value is $\sim(4e^2/h)\ hf \sim 25\ \mu$A for small-diameter SWNT. This corresponds to a current density of $j = 2.5 \times 10^9$ A/cm$^2$ for a 1 nm diameter tube. This is orders of magnitude larger than current densities found in present-day interconnects. This large current density can be attributed to the strong covalent bonding of the atoms in the tube. Unlike in metals, there are no low energy defects, dislocations, etc., that can easily lead to the motion of atoms in the conductor.

In addition to phonon scattering, scattering off of static disorder (defects, etc.) is also possible in metallic tubes. A number of sources of scattering have been identified, including physical bends in the tube [32] and [33] and localized electronic states created at defects along the tube [34]. One technique that can give direct information about these scattering centers is scanned gate microscopy (SGM). In this technique, a metallized AFM tip is used as a local gate to probe the conducting properties. Fig. 4 shows a SGM image of a metallic tube [34]. The dark features in the images correspond to locations of defects, which

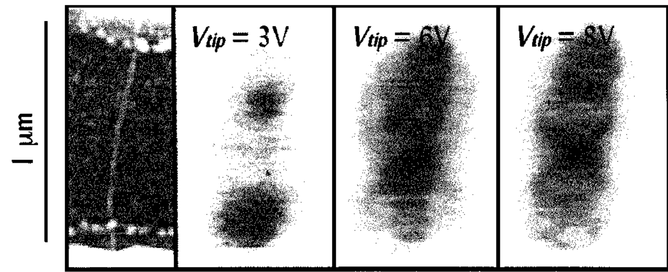



Fig. 4. Left panel: AFM image of a metallic SWNT. Other panels: Scanned gate microscopy of defects in the SWNT at different AFM tip voltages. The conductance through the SWNT is recorded as a function of the tip position. Resonant scattering at defect sites is indicated by rings of reduced conductance (dark) centered on the defects.

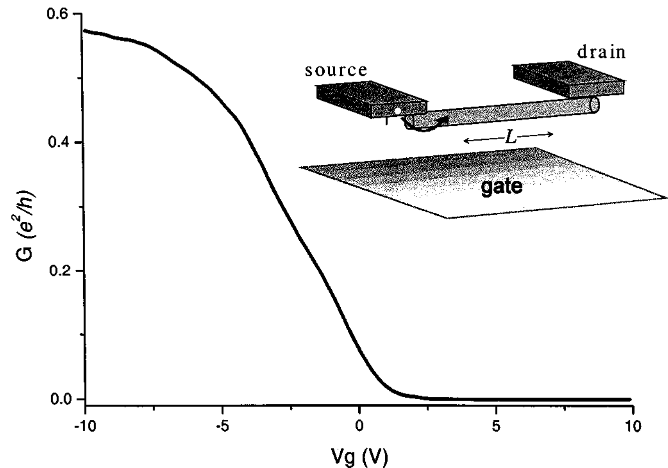



Fig. 5. Conductance $G$ versus gate voltage $V_g$ of a p-type semiconducting SWNT field effect transistor. The device geometry is shown schematically in the inset.

are conjectured to be associated with a bond-rotation defect in the nanotube. Measurements show that these defects are more common in tubes grown at lower temperatures (~700 °C). With proper control of the growth parameters, however, static defects can be minimized so that they are not an important source of scattering at room temperature.

## IV. ELECTRICAL PROPERTIES OF SEMICONDUCTING TUBES

Semiconducting behavior in nanotubes was first reported by Tans *et al.* in 1998 [5]. Fig. 5 shows a measurement of the conductance of a semiconducting SWNT as the gate voltage applied to the conducting substrate is varied. The tube conducts at negative $V_g$ and turns off with a positive $V_g$. The resistance change between the on and off state is many orders of magnitude. This device behavior is analogous to a p-type metal–oxide–semiconductor field-effect transistor (MOSFET), with the nanotube replacing Si as the semiconductor. At large positive gate voltages, n-type conductance is sometimes observed, especially in larger-diameter tubes [35] and [36]. The conductance in the n-type region is typically less than in the p-type region because of the work function of the Au electrodes. The Au Fermi level aligns with the valence band of the SWNT, making a p-type contact with a barrier for the injection of electrons.

Semiconducting nanotubes are typically p-type at $V_g = 0$ because of the contacts and also because chemical species, particularly oxygen, adsorb on the tube and act as weak p-type dopants. Experiments have shown that changing a tube's chemical environment can change this doping level—shifting the voltage at which the device turns on by a significant amount [37] and [38]. This has spurred interest in nanotubes as chemical sensors. Adsorbate doping can be a problem for reproducible device behavior, however. In air, a large hysteresis in $G$ versus $V_g$ is observed, with threshold voltage shifts of many volts common. In addition, the threshold voltage is very sensitive to the processing history of the device—for example, heating or exposure to UV radiation drives off oxygen [39], lowering the p-doping level of the device. Controlling adsorbate doping is an important challenge to be addressed. Recent work by the group at IBM has taken important steps in this direction [40].

Controlled chemical doping of tubes, both p- and n-type, has been accomplished in a number of ways. N-type doping was first done using alkali metals that donate electrons to the tube. This has been used to create n-type transistors [38], [41], [42], p-n junctions [43], and p-n-p devices [44]. Alkalai metals are not air-stable, however, so other techniques are under development, such as using polymers for charge-transfer doping [45]. While these techniques are progressing rapidly, we will concentrate here on tubes with no additional doping (beyond uncontrolled doping by adsorbates) and the carriers induced by the gate. For simplicity, we will further focus on the p-type conducting regime to get a sense of the basic parameters that characterize electrical transport.

In the data of Fig. 5, the conductance initially rises linearly with $V_g$ as additional holes are added to the nanotube. At higher gate voltages, the conductance stops increasing and instead is constant. This limiting conductance is due both to the tube and to the contact resistance between the metallic electrodes and to the tube. The value of this resistance can vary by orders of magnitude from device to device, but by annealing the contacts, on-state resistances of ~20–50 kΩ can be routinely obtained. In the regime where $G$ grows linear with $V_g$, the properties of the device can be described by the Drude-type relation $G = C'_g (V_g - V_{go}) \mu / L$, where $C'_g$ is the capacitance per unit length of the tube, $V_{go}$ is the threshold voltage, $\mu$ is the mobility. The capacitance per unit length of the tube can be estimated or obtained from other measurements [3], [4], [46]. Using this we can infer the mobility of the tube, $\mu$. We find typical mobilities of 1000–10 000 $cm^2$/V·s for CVD-grown tubes, with occasional devices having mobilities as high as 20 000 $cm^2$/V·s. This is significantly higher than the values reported to date in deposited nanotubes [25], [40], [47], [48]. It is also higher than the mobilities in Si MOSFETs, indicating than SWNTs are a remarkably high-quality semiconducting material.

As with metallic tubes, work has also been performed to investigate the nature of the scattering sites in nanotubes. Again, scanned probe techniques has been very useful. A scanned gate microscopy measurement is shown in Fig. 6(a). The tip was biased positively, to locally deplete the carriers (holes) underneath the tip. The bright spots in the image correspond to places where the AFM tip affected the conductance of the sample, producing a map of the barriers to conduction. This data shows that the conductance is limited by a series of potential barriers that the holes see as they traverse the tube. The barriers are likely due local inhomogeneities in the surface potential from adsorbed charges, etc., at or near the tube. At higher densities, however, little effect of the tip was seen, suggesting excellent transport properties. Electric force microscopy [49] can be used to directly probe the voltage drop along the length of the channel; the result is shown if Fig. 6(b). A linear voltage drop corresponding to a resistance of ~9 kΩ/$\mu$m is observed, implying a mean-free path of ~0.7 $\mu$m, comparable to the mean-free paths in metallic tubes. This result is consistent with the maximum conductances observed for semiconducting SWNTs ($G \sim e^2/h$ for 1-$\mu$m long tubes) and the high mobilities discussed above.

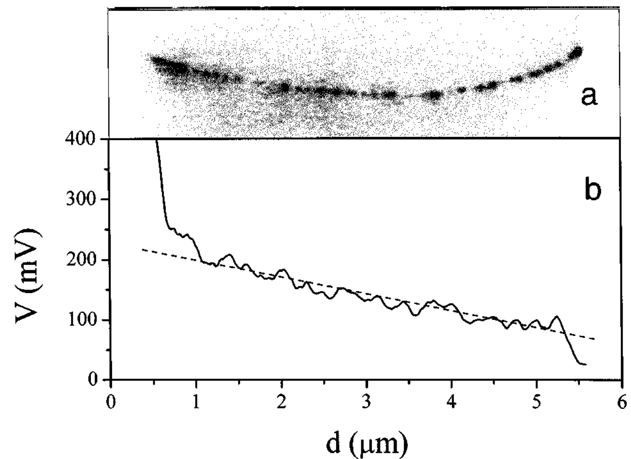



Fig. 6. (a) Scanned gate microscopy showing scattering sites in a p-type semiconducting SWNT. (b) Voltage drop along the length of the source–drain biased semiconducting SWNT, as determined by electric force microscopy. The slope of the voltage drop (dotted line) indicates a resistance per unit length of 9 kΩ/$\mu$m.

In order to maximize device performance, the tube gate capacitance $C'_g$ should be maximized. Most experiments to date have used gate oxide thicknesses of hundreds of millimicrons. More recently, researchers have investigated a number of ways to increase the gate coupling, such as using a very thin Al oxide gate [25] or using an electrolyte solution as a gate [26] and [27]. The latter is schematically shown in Fig. 7(a), with the resulting $I$–$V$ curves at different $V_g$s shown in Fig. 7(b). Standard FET behavior is seen; the current initially rises linearly with $V_{sd}$ and then becomes constant in the saturation region. The nanotube exhibits excellent characteristics, with a maximum transconductance, $dI/dVg = 20$ $\mu$A/V at $V_g = -0.9$ V. Normalizing this to the device width of ~2 nm, this gives a transconductance per unit width of ~10-mS/$\mu$m. This is significantly better than current-generation MOSFETs.

The properties of semiconducting SWNTs given above are quite remarkable. Perhaps most surprising is the high mobilities obtained given the small channel width and the simplicity of the fabrication methods employed. This is largely due to the lack of surface states in these devices. As is well known from bulk semiconductors, surface states generally degrade the operating properties of the device, and controlling them is one of the key technological challenges to device miniaturization. A SWNT solves the surface state problem in an elegant fashion. First, it

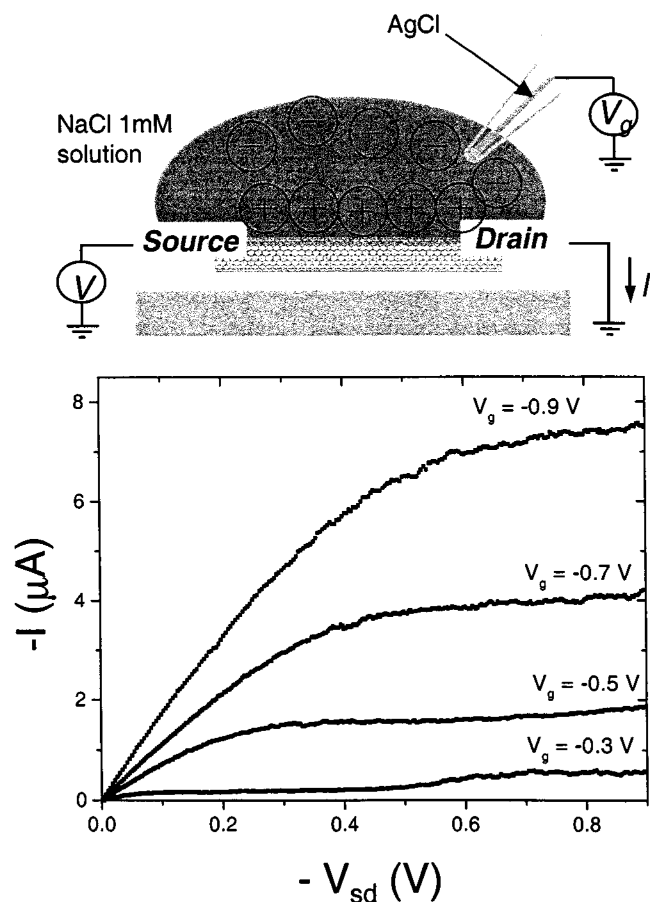



Fig. 7. $I$–$V$ characteristics at different $V_g$s for a p-type SWNT FET utilizing an electrolyte gate. A schematic of the measurement geometry is also shown.

begins with a 2-D material with no chemically reactive dangling bonds. It then rids itself of the problem of edges by using the topological trick of rolling itself into a cylinder—which has no edges.

## V. Challenges and Future Prospects

The above results show that single nanotube devices possess excellent properties. Metallic tubes have conductivities and current densities that meet or exceed the best metals, and semiconducting tubes have mobilities and transconductances that meet or exceed the best semiconductors. This clearly make them very promising candidates for electronic applications. Opportunities also exist for integrating nanotube electronics with other chemical, mechanical, or biological systems. For example, nanotube electronic devices function perfectly well under biological conditions (i.e., salty water) and have dimensions comparable to typical biomolecules (e.g., DNA, whose width is approximately 2 nm). This makes them an excellent candidate for electrical sensing of individual biomolecules. The are also a host of other device geometries beyond the simple wire and FET structures described above that are under exploration. Examples include the p-n and p-n-p devices mentioned previously [43] and [44], nanotube/nanotube junctions [50]–[52], and electromechanical devices [53] and [54].

Much more challenging is the issue of device manufacturability. Although a great deal of work has been done, the progress to date has been modest. For example, in tube synthesis, the diameter of the tubes can be controlled, but not the chirality. As a result, the tubes are a mixture of metal and semiconductors. In CVD, the general location for tube growth can be controlled by patterning the catalyst material, but the number of tubes and their orientation relative to the substrate are still not well defined. Furthermore, the high growth temperature (900 °C) for CVD tubes is incompatible with many other standard Si processes. The alternative approach, depositing tubes on a substrate after growth, avoids this high temperature issue but suffers from the chirality and positioning limitations discussed above. Furthermore, the wet processing of the tubes may degrade their electrical properties. Efforts are underway to address these issues. For example, techniques to guide tubes to desired locations during growth or deposition using electric fields [55] and/or surface modification [24] are being explored, with some success.

To date, there are no reliable, rapid, and reproducible approaches to creating complex arrays of nanotube devices. This manufacturing issue is by far the most significant impediment to using nanotubes in electronics applications. While there has been significant fanfare around "circuits" made with nanotubes, (see, e.g., the "Breakthrough of the Year" for 2001 in *Science* magazine), in reality the accomplishments to date are a far cry from anything that would impress a device engineer or circuit designer. However, there appear to be no fundamental barriers to the development of a technology. The science of nanotubes has come a long way in five years. With the involvement of the engineering community, perhaps the technology of nanotubes will see similar progress in the next five.

## Acknowledgment

The authors would like thank their many collaborators at Cornell University, Ithaca, NY, Harvard University, Cambridge, MA, and at the University of California at Berkeley who participated in the work described here.

## References

[1] S. Iijima and T. Ichihashi, "Single-shell carbon nanotubes if 1-Nm diameter," *Nature*, vol. 363, pp. 603–605, 1993.
[2] D. S. Bethune, C. H. Kiang, M. S. Devries, G. Gorman, R. Savoy, J. Vazquez, and R. Beyers, "Cobalt-catalyzed growth of carbon nanotubes with single-atomic-layerwalls," *Nature*, vol. 363, pp. 605–607, 1993.
[3] S. J. Tans, M. H. Devoret, H. Dai, A. Thess, R. E. Smalley, L. J. Georliga, and C. Dekker, "Individual single-wall carbon nanotubes as quantum wires," *Nature*, vol. 386, pp. 474–477, 1997.
[4] M. Bockrath, D. H. Cobden, P. L. McEuen, N. G. Chopra, A. Zettl, A. Thess, and R. E. Smalley, "Single-electron transport in ropes of carbon nanotubes," *Science*, vol. 275, pp. 1922–1925, 1997.
[5] S. J. Tans, R. M. Verschueren, and C. Dekker, "Room temperature transistor based on a single carbon nanotube," *Nature*, vol. 393, pp. 49–52, 1998.
[6] N. Hamada, S. Sawada, and A. Oshiyama, "New one-dimensional conductors—Graphitic microtubules," *Phys. Rev. Lett.*, vol. 68, pp. 1579–1581, 1992.
[7] R. Saito, M. Fujita, G. Dresselhaus, and M. S. Dresselhaus, "Electronic structure of chiral graphene tubules," *Appl. Phys. Lett.*, vol. 60, pp. 2204–2206, 1992.
[8] T. W. Odom, H. Jin-Lin, P. Kim, and C. M. Lieber, "Atomic structure and electronic properties of single-walled carbon nanotubes," *Nature*, vol. 391, pp. 62–64, 1998.

[9] J. W. G. Wildoer, L. C. Venema, A. G. Rinzler, R. E. Smalley, and C. Dekker, "Electronic structure of atomically resolved carbon nanotubes," *Nature*, vol. 391, pp. 59–62, 1998.

[10] S. Datta, *Electronic Transport in Mesoscopic Systems*. Cambridge, MA: Cambridge Univ. Press, 1995.

[11] C. Dekker, "Carbon nanotubes as molecular quantum wires," *Physics Today*, vol. 52, p. 22, 1999.

[12] J. Nygard, D. H. Cobden, M. Bockrath, P. L. McEuen, and P. E. Lindelof, "Electrical transport measurements on single-walled carbon nanotubes," *Appl. Phys. A, Solids Surf.*, vol. A69, pp. 297–304, 1999.

[13] Z. Yao, C. Dekker, and P. Avouris, "Electrical transport through single-wall carbon nanotubes," in *Topics in Applied Physics*, M. S. Dresselhaus, G. Dresselhaus, and P. Avouris, Eds. Berlin, Germany: Springer-Verlag, 2001, vol. 80, pp. 147–171.

[14] N. R. Franklin and H. Dai, "An enhanced CVD approach to extensive nanotube networks with directionality," *Adv. Mater.*, vol. 12, pp. 890–894, 2000.

[15] A. Thess, R. Lee, P. Nikolaev, H. Dai, P. Petit, J. Robert, X. Chunhui, L. Young Hee, K. Seong Gon, A. G. Rinzler, D. T. Colbert, G. E. Scuseria, D. Tombnek, J. E. Fischer, and R. E. Smalley, "Crystalline ropes of metallic carbon nanotubes," *Science*, vol. 273, pp. 483–487, 1996.

[16] J. Liu, A. G. Rinzler, H. Dai, J. H. Hafner, R. K. Bradley, P. J. Boul, A. Lu, T. Iverson, K. Shelimov, C. B. Huffman, F. Rodriguez-Macias, Y.-S. Shon, T. R. Lee, D. T. Colbert, and R. E. Smalley, "Fullerene pipes," *Science*, vol. 280, pp. 1253–1256, 1998.

[17] J. Chen, M. A. Hamon, H. Hu, Y. Chen, A. M. Rao, P. C. Eklund, and R. C. Haddon, "Solution properties of single-walled carbon nanotubes," *Science*, vol. 282, pp. 95–98, 1998.

[18] E. T. Mickelson, C. B. Huffman, A. G. Rinzler, R. E. Smalley, R. H. Hauge, and J. L. Margrave, "Fluorination of single-wall carbon nanotubes," *Chem. Phys. Lett.*, vol. 296, pp. 188–194, 1998.

[19] J. Chen, A. M. Rao, S. Lyuksyutov, M. E. Itkis, M. A. Hamon, H. Hu, R. W. Cohn, P. C. Eklund, D. T. Dolbert, R. E. Smalley, and R. C. Haddon, "Dissolution of full-length single-walled carbon nanotubes," *J. Phys. Chem. B*, vol. 105, pp. 2525–2528, 2001.

[20] S. Niyogi, H. Hu, M. A. Hamon, P. Bhowmik, B. Zhao, S. M. Rozenzhak, J. Chen, M. E. Itkis, M. S. Meier, and R. C. Haddon, "Chromatographic purification of soluble single-walled carbon nanotubes (s-SWNT's)," *J. Amer. Chem. Soc.*, vol. 123, pp. 733–734, 2001.

[21] J. Kong, H. T. Soh, A. Cassell, C. F. Quate, and H. Dai, "Synthesis of single single-walled carbon nanotubes on patterned silicon wafers," *Nature*, vol. 395, p. 878, 1998.

[22] Y. Li, W. Kim, Y. Zhang, M. Rolandi, D. Wang, and H. Dai, "Growth of single-walled carbon nanotubes from discrete catalytic nanoparticles of various sizes," *J. Phys.Chem. B*, vol. 105, p. 11 424, 2001.

[23] C. L. Cheung, A. Kurtz, H. Park, and C. M. Lieber, "Diameter controlled synthesis of carbon nanotubes," J. Phys. Chem. B, vol. 105, 2002, to be published.

[24] J. Liu, M. J. Casavant, M. Cox, D. A. Walters, P. Boul, L. Wei, A. J. Rimberg, K. A. Smith, D. T. Colbert, and R. E. Smalley, "Controlled deposition of individual single-walled carbon nanotubes on chemically functionalized templates," *Chem. Phys. Lett.*, vol. 303, pp. 125–129, 1999.

[25] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, "Logic circuits with carbon nanotube transistors," *Science*, vol. 294, pp. 1317–1320, 2001.

[26] M. Kruger, M. R. Buitelaar, T. Nussbaumer, C. Schonenberger, and L. Forro, "Electrochemical carbon nanotube field-effect transistor," *Appl. Phys. Lett.*, vol. 78, pp. 1291–1293, 2001.

[27] S. Rosenblatt, Y. Yaish, J. Park, J. Gore, and P. L. McEuen, "High performance electrolyte gates carbon nanotube transistors," .

[28] L. Wenjie, M. Bockrath, D. Bozovic, J. H. Hafner, M. Tinkham, and P. Hongkun, "Fabry–Perot interference in a nanotube electron waveguide," *Nature*, vol. 411, pp. 665–669, 2001.

[29] J. Kong, E. Yenilmez, T. W. Tombler, W. Kim, H. Dai, R. B. Laughlin, L. Liu, C. S. Jayanthi, and S. Y. Wu, "Quantum interference and ballistic transmission in nanotube electron waveguides," *Phys. Rev. Lett.*, vol. 87, pp. 106 801/1–106 891/4, 2001.

[30] A. Bachtold, M. S. Fuhrer, S. Plyasunov, M. Forero, E. H. Z. Anderson, Z. A. Zettl, and P. L. McEuen, "Scanned probe microscopy of electronic transport in carbon nanotubes," *Phys. Rev. Lett.*, vol. 84, pp. 6082–6085, 2000.

[31] Z. Yao, C. L. Kane, and C. Dekker, "High-field electrical transport in single-wall carbon nanotubes," *Phys. Rev. Lett.*, vol. 84, pp. 2941–2944, 2000.

[32] H. W. C. Postma, M. de Jonge, and C. Dekker, "Electrical transport through carbon nanotube junctions created by mechanical manipulation," *Phys. Rev. B, Condens. Matter*, vol. 62, pp. R10653–R10656, 2000.

[33] D. Bozovic, M. Bockrath, J. H. Hafner, C. M. Lieber, P. Hongkun, and M. Tinkham, "Electronic properties of mechanically induced kinks in single-walled carbon nanotubes," *Appl. Phys. Lett.*, vol. 78, pp. 3693–3695, 2001.

[34] M. Bockrath, L. Wenjie, D. Bozovic, J. H. Hafner, C. M. Lieber, M. Tinkham, and P. Hongkun, "Resonant electron scattering by defects in single-walled carbon nanotubes," *Science*, vol. 291, pp. 283–285, 2001.

[35] J. Park and P. L. McEuen, "Formation of a p-type quantum dot at the end of an n-type carbon nanotube," *Appl. Phys. Lett.*, vol. 79, pp. 1363–1365, 2001.

[36] A. Javey, M. Shim, and H. Dai, "Electrical properties and devices of large-diameter single-walled carbon nanotubes," *Appl. Phys. Lett.*, vol. 80, p. 1064, 2002.

[37] J. Kong, N. R. Franklin, C. Zhou, M. G. Chapline, S. Peng, K. Cho, and H. Dai, "Nanotube molecular wires as chemical sensors," *Science*, vol. 287, p. 622, 2000.

[38] V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, "Carbon nanotube inter- and intramolecular logic gates," *Nano Lett.*, vol. 1, pp. 453–456, 2001.

[39] R. J. Chen, N. R. Franklin, K. Jing, C. Jien, T. W. Tombler, Z. Yuegang, and D. Hongjie, "Molecular photodesorption from single-walled carbon nanotubes," *Appl. Phys. Lett.*, vol. 79, pp. 2258–2260, 2001.

[40] R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. K. Chan, J. Tersoff, and P. Avouris, "Ambipolar electrical transport in semiconducting single-wall carbon nanotubes," *Phys. Rev.Lett.*, vol. 87, p. 256 805, 2001.

[41] M. Bockrath, J. Hone, A. Zettl, P. L. McEuen, A. G. Rinzler, and R. E. Smalley, "Chemical doping of individual semiconducting carbon-nanotube ropes," *Phys. Rev. B, Condens. Matter*, vol. 61, pp. R10606–R10608, 2000.

[42] J. Kong, C. Zhou, E. Yenilmez, and H. Dai, "Alkaline metal-doped n-type semiconducting nanotubes as quantum dots," *Appl. Phys. Lett.*, vol. 77, pp. 3977–3979, 2000.

[43] C. Zhou, J. Kong, E. Yenilmez, and H. Dai, "Modulated chemical doping of individual carbon nanotubes," *Science*, vol. 290, pp. 1552–1555, 2000.

[44] J. Kong, J. Cao, and H. Dai, "Chemical profiling of single nanotubes: Intramolecular p–n–p junctions and on-tube single-electron transistors," *Appl. Phys. Lett.*, vol. 80, p. 73, 2002.

[45] J. Kong and H. Dai, "Full and modulated chemical gating of individual carbon nanotubes by organic amine compounds," *J. Phys. Chem. B*, vol. 105, p. 2890, 2001.

[46] D. H. Cobden, M. Bockrath, P. L. McEuen, A. G. Rinzler, and R. E. Smalley, "Spin splitting and even–odd effects in carbon nanotubes," *Phys. Rev. Lett.*, vol. 81, pp. 681–684, 1998.

[47] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single- and multi-wall carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 73, pp. 2447–2479, 1998.

[48] P. L. McEuen, M. Bockrath, D. H. Cobden, Y.-G. Yoon, and S, G. Louie, "Disorder, pseudospins, and backscattering in carbon nanotubes," *Phys. Rev. Lett.*, vol. 83, p. 5098, 1999.

[49] A. Bachtold, M. S. Fuhrer, S. Plyasunov, M. Forero, E. H. Anderson, A. Zettl, and P. I. McEuen, "Scanned probe microscopy of electronic transport in carbon nanotubes," *Phys. Rev. Lett.*, vol. 84, pp. 6082–6085, 2000.

[50] Z. Yao, H. W. C. Postma, L. Balents, and C. Dekker, "Carbon nanotube intramolecular junctions," *Nature*, vol. 402, p. 273, 1999.

[51] J. Lefebvre, R. D. Antonov, M. Radosavljevic, J. F. Lynch, M. Llaguno, and A. T. Johnson, "Single-wall carbon nanotube based devices," *Carbon*, vol. 38, pp. 1745–1749, 2000.

[52] M. S. Fuhrer, J. Nygård, L. Shih, M. Forero, Y.-G. Yoon, M. S. C. Mazzoni, H. J. Choi, J. Ihm, S. G. Louie, Z. A. Zettl, and P. L. McEuen, "Crossed nanotube junctions," *Science*, vol. 288, pp. 494–497, 2000.

[53] T. Rueckes, K. Kim, E. Joselevich, G. Y. Tseng, C. L. Cheung, and C. M. Lieber, "Carbon nanotube-based nonvolatile random access memory for molecular computing," *Science*, vol. 289, pp. 94–97, 2000.

[54] T. W. Tombler, Z. Chongwu, L. Alxseyev, K. Jing, D. Hongjie, L. Lei, C. S. Jayanthi, T. Meijie, and W. Shi-Yu, "Reversible electromechanical characteristics of carbon nanotubes under local-probe manipulation," *Nature*, vol. 405, pp. 769–772, 2000.

[55] Y. Zhang, A. Chang, J. Cao, Q. Wang, W. Kim, Y. Li, N. Morris, E. Yenilmez, J. Kong, and H. Dai, "Electric-field-directed growth of aligned single-walled carbon nanotubes," *Appl. Phys. Lett.*, vol. 79, pp. 3155–3157, 2001.

**Paul L. McEuen** was born in Norman, OK, in 1963. He received the B.S. degree in engineering physics from the University of Oklahoma in 1985 and the Ph.D.degree in applied physics from Yale University, New Haven, CT, in 1991.

He was a Postdoctoral Researcher at the Massachusetts Institute of Technology, Cambridge, before joining the University of California at Berkeley in 1992, where he was an Assistant Professor and later Associate Professor of physics and a researcher at LBNL. In 2001, he joined the faculty of Cornell University, Ithaca, NY, as a Professor of physics. His research examines the science and technology of nanostructures, and has included studies of nanotubes, quantum dots, and single molecules. He also develops advanced measurement techniques to probe nanometer-scale systems.

**Michael S. Fuhrer** received the B.S. degree in physics from the University of Texas at Austin in 1990 and the Ph.D. degree in physics from the University of California at Berkeley in 1998.

Since 2000, he has been an Assistant Professor of physics at the University of Maryland, College Park. His research interests lie in the electronic and electromechanical properties of nanostructures, including carbon nanotubes, nanowires, and new two-dimensional nanostructures.

**Hongkun Park** was born in Seoul, Korea, in 1967. He received the B.S. degree in chemistry from Seoul National University, Seoul, Korea, in 1990 and the Ph.D. degree in physical chemistry from Stanford University, Stanford, CA, in 1996.

Since 1999, he has been with the Department of Chemistry and Chemical Biology at Harvard University, Cambridge, MA, as an Assistant Professor. His research interests lie in the physics and chemistry of nanostructured materials, specifically: 1) to study electrical properties of individual molecules, clusters, carbon nanotubes, and their arrays and 2) to develop synthetic schemes for transition–metal–oxide nanostructures and to study their electronic and magnetic properties.

nature nanotechnology

REVIEW ARTICLE

PUBLISHED ONLINE: 29 NOVEMBER 2009 | DOI: 10.1038/NNANO.2009.355

# Nanotube electronics for radiofrequency applications

Chris Rutherglen, Dheeraj Jain and Peter Burke*

**Electronic devices based on carbon nanotubes are among the candidates to eventually replace silicon-based devices for logic applications. Before then, however, nanotube-based radiofrequency transistors could become competitive for high-performance analogue components such as low-noise amplifiers and power amplifiers in wireless systems. Single-walled nanotubes are well suited for use in radiofrequency transistors because they demonstrate near-ballistic electron transport and are expected to have high cut-off frequencies. To achieve the best possible performance it is necessary to use dense arrays of semiconducting nanotubes with good alignment between the nanotubes, but techniques that can economically manufacture such arrays are needed to realize this potential. Here we review progress towards nanotube electronics for radiofrequency applications in terms of device physics, circuit design and the manufacturing challenges.**

The potential to exploit single-walled carbon nanotubes in advanced electronics has been a major goal in nanotechnology for over a decade[1,2]. This interest stems from the fact that carbon nanotubes offer a combination of small size, high mobility[3,4], large current density and low intrinsic capacitance: moreover, their intrinsic cut-off frequency is expected to be high. Although the long-term goal of nanotube researchers has been to replace digital CMOS devices made from silicon, and therefore to "extend Moore's law", a more realistic point of insertion into the market may be high-performance analogue radiofrequency (RF) devices, where manufacturing tolerances are relaxed and the performance metrics required for commercial systems are more suited to the materials and device properties of nanotubes. To realize this potential, it must be possible to economically manufacture dense aligned arrays of all-semiconducting nanotubes.

The use of massively parallel nanotube-based field-effect transistors (FETs) for applications such as mobile communication devices and radar is at present being investigated in both academic and industrial laboratories. So far, numerous nanotube-based FETs have been demonstrated using both single nanotubes and thin-film transistors made from mixtures of semiconducting and metallic nanotubes[5]. (The nanotubes in these devices can either be aligned or randomly oriented.) However, to achieve the highest performance, the nanotubes must be aligned at a high density (Fig. 1). Otherwise, the mobility is degraded from that of a pristine nanotube, and the fringe-field capacitance degrades the cut-off frequency by up to two orders of magnitude[6]. For this reason, the manufacturability of aligned arrays is very important, and several techniques have been investigated to solve the problems of nanotube alignment and purification: the two main techniques are 'grow in place' and 'deposition from solution'.

It has been proposed that nanotube-based FETs could, in principle, operate at frequencies well into the terahertz regime[6–11]. However, as it might not be possible to economically manufacture the perfectly dense perfectly aligned arrays containing only semiconducting nanotubes that are needed to achieve this level of performance, it is important to benchmark trade-offs that result from using less-than-perfect arrays. An intriguing aspect of nanotube-based FETs is a predicted inherent linearity[12], which is critically important for wireless communication systems. To confirm and quantify these and other device properties under realistic operating conditions, it is important to fabricate, test and demonstrate devices with high-density, aligned, all-semiconducting nanotubes in a scalable process, and to demonstrate such devices in actual working radio systems applications.

Here we review the progress so far in manufacturing, discuss the predicted and measured device properties as a function of manufacturing tolerances, and consider the implications for applications of single-walled nanotubes in analogue (as opposed to digital) RF devices and, ultimately, RF systems applications.

## Grow in place by chemical vapour deposition

The most widely used method for growing single-walled nanotubes directly onto a substrate has been chemical vapour deposition (CVD). In general, a substrate holding metal catalyst particles is placed within a furnace with a flow of carbon feedstock gas and hydrogen gas at temperatures upwards of 900 °C. In such an environment, carbon nanotubes will grow from the catalyst particles with a diameter that is related to the size of these particles. To obtain aligned nanotubes during the CVD growth, multiple methods have been used to guide the alignment, such as applied electric fields[13,14], the gas flow[15–18] and interactions with the substrate. Of these, the most successful for obtaining highly dense perfectly aligned arrays of nanotubes has been surface-guided growth on single-crystal substrates such as sapphire or quartz[19–25]. Although the basic alignment mechanism remains unclear, it is assumed to involve the interactions between the nanotubes and the substrate's atomic steps, nanofacets or crystallographic lattice — or a mixture of these. Nanotube lengths of greater than 100 μm, linear densities of 10 nanotubes $\mu m^{-1}$ (with peak values ~50 nanotubes $\mu m^{-1}$) and alignment within <0.01° have been achieved (Fig. 1c). Furthermore, procedures for transferring the aligned arrays to other substrates, such as $SiO_2$, or flexible substrates have been developed[26]. These techniques allow heterogeneous integration of aligned single-walled nanotubes with other materials that would not otherwise survive the high temperatures involved with the CVD nanotube growth process.

Nanotubes produced by the methane CVD method typically yield a mixture of two-thirds semiconducting nanotubes and one-third metallic nanotubes. The presence of the metallic nanotubes in parallel with the semiconducting nanotubes degrades device performance, especially the on/off ratio and the output resistance. Individual nanotube-based FETs have demonstrated on/off

Integrated Nanosystems Research Facility, Departmental of Electrical Engineering and Computer Science, University of California, Irvine, California 92697, USA. *e-mail: pburke@uci.edu



© 2009 Macmillan Publishers Limited. All rights reserved

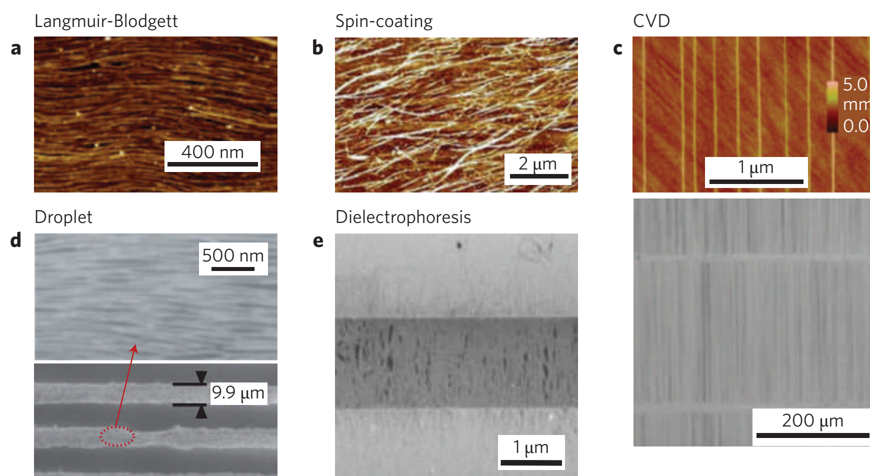



**Figure 1 | Different ways to align nanotubes.** To make high-frequency field-effect transistors from single-walled nanotubes (SWNTs), the nanotubes must be aligned, and they must also be long enough to span the source–drain channel. **a**, The Langmuir-Blodgett method can align SWNTs with a density of 30 nanotubes μm$^{-1}$, as shown in this atomic force microscopy image. Reproduced with permission from ref. 42 (© 2007 ACS). **b**, The spin-coating method is capable of aligning 10 nanotubes μm$^{-2}$, and an alignment of less than 10° of the radial axis, as shown in this atomic force microscopy image. Reproduced with permission from ref. 51 (© 2008 AAAS). **c**, Growing SWNTs by CVD on a single-crystal quartz substrate yields a high degree of alignment (<0.01°), as seen in the atomic force microscopy image (top). This method also produces nanotubes with lengths greater than 100 μm between the pair of catalyst lines, as shown in the scanning electron microscopy image (bottom). Reproduced with permission from ref. 29 (© 2009 ACS). **d**, The evaporating-droplet method produces densities of 10–20 nanotubes μm$^{-1}$, and alignment of less than 5°, as shown in these scanning electron microscopy images. Reproduced with permission from ref. 52 (© 2008 ACS). **e**, Dielectrophoresis uses the electric field to attract and align SWNTs between a pair of electrodes, as seen in this scanning electron microscopy image. Reproduced with permission from ref. 43 (© 2008 AIP).

ratios $>10^6$, but this ratio is much lower for combinations of metallic and semiconducting nanotubes. Although a degradation in the on/off ratio is acceptable for analogue RF applications (which relaxes the manufacturing requirements for analogue devices compared with those for digital devices), the presence of the metallic nanotubes also reduces the output resistance, which lowers the gain and frequency of operation, as discussed below. Therefore, it is necessary to devise strategies to selectively remove the metallic nanotubes while preserving (as much as possible) the semiconducting nanotubes.

Various gas-phase or plasma-etching methods have been developed to selectively remove metallic nanotubes[27,28]. Some of these methods can be incorporated into the growth process itself[29,30], and a combination of ethanol/methanol carbon feedstock mixture and copper nanoparticles as the catalyst was recently used to selectively grow >95% semiconducting nanotubes with a narrow diameter distribution and on/off ratios up to 85 (ref. 29). This selective growth is thought to be due to the $OH^-$ radical from methanol selectively etching the metallic nanotubes during the growth owing to their smaller ionization potential compared with the semiconducting variety.

Using such preferential growth, one can further enhance the on/off current ratio by post-growth removal of the metallic nanotubes. One such method[27] involves the selective etching by hydrocarbonation of metallic nanotubes with diameters between ~1.3 and 1.6 nm using a 400 °C methane plasma treatment to achieve on/off ratios of $10^4$–$10^5$. It is found that nanotubes having a diameter smaller than this range are indiscriminately etched regardless of being metallic or semiconducting, whereas those with larger diameters are not affected at all. This general processing method has the advantage that it is scalable and compatible with other traditional semiconductor processing techniques, although some semiconducting nanotubes are also damaged in the process.

'Wet etching' of metallic nanotubes has also been demonstrated. The process originates from the selective reaction of diazonium salts with the sidewalls of the nanotubes to significantly perturb their electronic and optical properties[31–33]. On/off current ratios are found to improve to $10^4$.

The electrical breakdown method is a post-growth treatment that involves selectively 'burning off' metallic nanotubes by applying a strong gate-bias to deplete or turn off the semiconducting nanotube, thus forcing the current though the metallic nanotubes[34]. By ramping up the drain–source voltage, typically to greater than 30 V, it is possible to burn off the metallic nanotubes in the presence of oxygen. This process has been shown to improve the on/off current ratio upwards of $10^5$, but this improvement comes at the cost of decreasing the pre-breakdown mobility owing to the inadvertent damaging of the semiconducting nanotubes as a result of

**Table 1 | Ideal parameter values for making a high-frequency field-effect transistor from single-walled nanotubes.**

| Property/parameter | Target value or range | Justification |
|---|---|---|
| Diameter | 1.5–2.0 nm | Current is largest in this range[54-55]. |
| Chirality | Semiconducting and same (*n*,*m*) | To obtain identical transport properties. |
| Purity | >99% semiconducting nanotubes | No metallic nanotubes for high gain and high $f_{max}$. |
| Length | >1 μm | Nanotube length must be longer than the intended channel length. |
| Density | >10 nanotubes μm$^{-1}$ | Reduces the parasitic capacitance per nanotube; increases current carrying capacity; improves impedance matching. |
| Alignment | All parallel | Results in higher transconductance and denser nanotube packing. |
| Uniformity | Wafer scale | Essential for large-scale processing. |



© 2009 Macmillan Publishers Limited. All rights reserved

the Joule heating produced by adjacent metallic nanotubes. Such reduction in mobility has been found to result in a post-breakdown mobility of up to half its pre-breakdown value for the standard two-thirds semiconductor/one-third metallic mix with densities of ~10 nanotubes $\mu m^{-1}$ (refs 35–38). As the density is further increased and the distance between nanotubes becomes smaller, one would anticipate this collateral damage to adjacent nanotubes to be even more severe. From the scalability perspective, one would face the additional challenge of applying the necessary high voltage to each device on the wafer: an alternative approach that relies on microwaves[39] or light[40] to selectively burn off the metallic nanotubes has had some limited success.

## Deposition from solution

Radiofrequency FETs can also be made using the 'deposition from solution' technique. A variety of techniques have been developed to sort as-produced single-walled nanotubes: these include selective chemistry, chromatographic separation and electrophoretic separation (see ref. 41 for a review). Using these techniques, or a combination of them, in the near future it should be feasible to prepare a solution of nanotubes in which all the nanotubes have the same length and the same chirality. (The chirality of a nanotube is denoted by two integers $(n,m)$ which define the direction in which a hypothetical sheet of graphene would be rolled up to form that nanotube, and which also determine the diameter of the nanotube and whether it is metallic or semiconducting.)

When sorting nanotubes for applications in electronics the key challenges are: the economy of the process; the ability to sort large diameter (>1.5 nm) nanotubes; and the ability to sort sufficiently long nanotubes (ideally >1 μm) so that their length is longer than the source–drain spacing. Once these challenges (which do not seem to be insurmountable) have been solved, the remaining challenges will include learning how to deposit and assemble the nanotubes into an aligned array, and understanding how residual surfactants influence the electronic properties of the array once it has been assembled. (Nanotubes tend to be insoluble, so it is usually necessary to functionalize them first to make them soluble before they can be used in 'deposition from solution' methods.) Progress in these areas is reviewed below.

In the Langmuir-Blodgett technique a solution of nanotubes is spread on top of water in a Langmuir-Blodgett trough (in much the same way that oil spreads to form a slick on water), and movable barriers in the trough are used to subject the sample to cycles of compression and retraction, which results in the formation of a self-assembled monolayer of nanotubes. The nanotubes are then transferred onto a solid substrate by successively dipping the substrate through the monolayer. This method[42] has yielded linearly aligned tubes with packing densities of more than 30 nanotubes $\mu m^{-1}$ (Fig. 1a), and the process is conceivably scalable to wafer-scale processing.

Nanotubes can be aligned using a.c. electric fields and then deposited between two closely spaced electrodes using dielectrophoresis[43–46] (Fig. 1e). A disadvantage of this process is its tendency to preferentially accumulate metallic nanotubes owing to their stronger polarizability compared with semiconducting nanotubes[47–50]. The other challenges include scaling up the process for wafer-scale production and combating the tendency of the nanotubes to form bundles during deposition.

Spin coating is a simple technique that involves spinning a wafer (usually made of silicon) at high speeds, and dripping a solution of nanotubes onto it so that they are deposited in a radially aligned pattern[51]. Although on/off ratios of $>10^5$ have been achieved, the devices have a low on-state current owing to the very large sheet resistance of the nanotube film. So far the densities obtained have been ~10 nanotubes $\mu m^{-2}$ with moderate alignment (within ~10° of the radial axis[51]; Fig. 1b). (For randomly aligned nanotubes, researchers tend to quote areal rather than linear densities.)

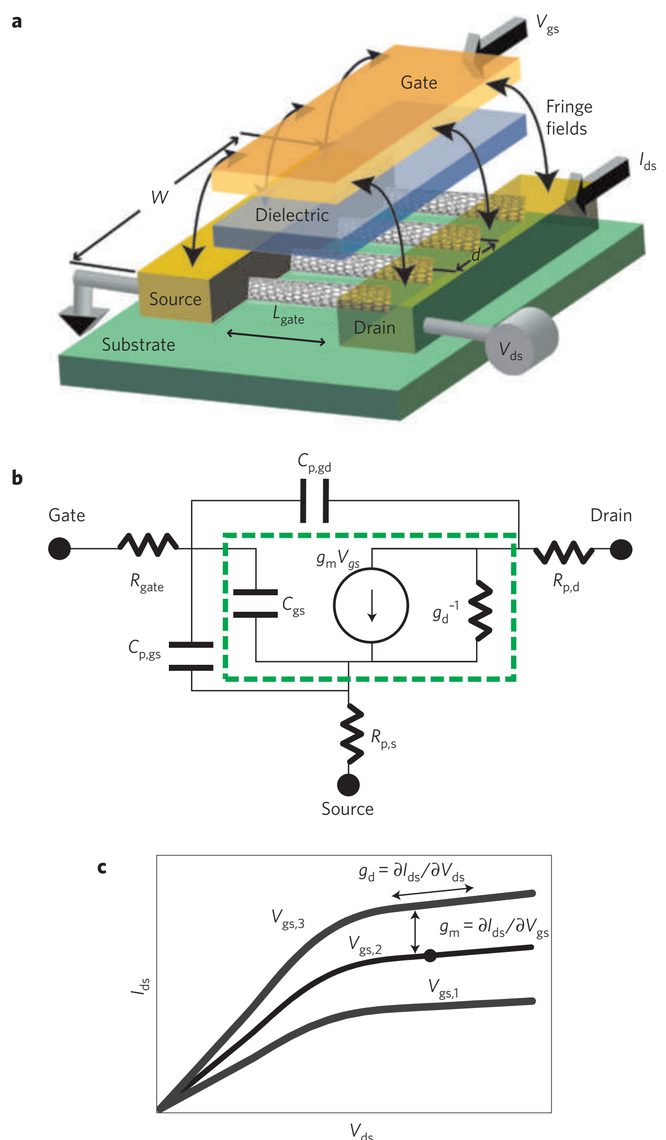



**Figure 2 | The nanotube field-effect transistor. a**, Schematic showing a FET in which the channel is an array of single-walled nanotubes: $W$ is the gate width, $L_{gate}$ is the gate length, $d$ is the pitch (or spacing) of the nanotubes, $V_{gs}$ and $V_{ds}$ are the gate–source and drain–source voltages, and $I_{ds}$ is the drain–source current. For RF-FETs, aligned arrays of nanotubes are needed to improve the impedance matching and increase the transconductance, the on-state current and the power density of the device. The fringe electrical fields from the gate to the source and drain give rise to the parasitic capacitance. **b**, A small-signal equivalent circuit for a nanotube-based FET where $g_m$ is the transconductance, $C_{gs}$ the intrinsic gate capacitance, and $g_d$ the channel conductance (which can be significant if metallic nanotubes are present). These components encompass the 'intrinsic' portion of the device. The components outside the dashed line are parasitic elements: $C_{p,gs}$ and $C_{p,gd}$ are the gate–source and gate–drain parasitic capacitances, $R_{p,s}$ and $R_{p,d}$ are parasitic resistances for the source and drain, and $R_{gate}$ is the resistance of the gate electrode. **c**, Schematic showing how the current through a nanotube transistor $I_{ds}$ varies with the voltage across the transistor $V_{ds}$ at three different values of the gate voltage $V_{gs}$. In practical applications the transistor is operated in the saturation regime at the values of $V_{ds}$ and $V_{gs}$ that give the optimum performance for a particular application (such as the highest gain or lowest noise). For d.c. voltages, the transconductance $g_m$ depends on how $I_{ds}$ changes with respect to the changes in $V_{gs}$, whereas the channel conductance $g_d$ depends on how $I_{ds}$ changes with respect to the changes in $V_{ds}$.



© 2009 Macmillan Publishers Limited. All rights reserved

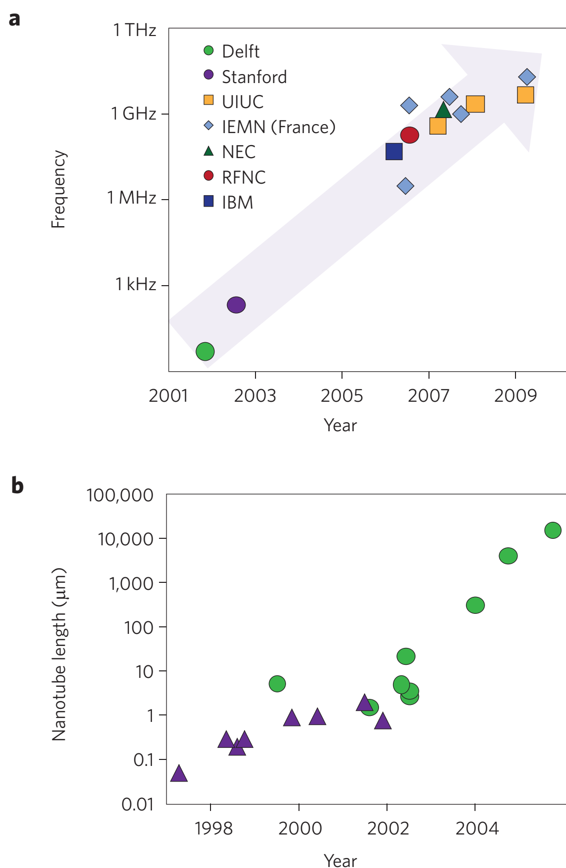



**Figure 3 | Improvements over time. a**, Maximum operating frequency (on a log scale) versus year for nanotube FETs. The maximum ring-oscillation frequency is plotted for the early work at Delft[69], Stanford[70] and IBM[71], and the cut-off frequency is plotted for the later work at RF Nano Corporation (RFNC)[60], NEC[72], Institut d'Electronique, de Microélectronique et de Nanotechnologie (IEMN)[68,73–75,77] and the University of Illinois at Urbana-Champaign (UIUC)[35,63,76]. **b**, Length of individual single-walled nanotubes (on a log scale) produced by laser ablation (purple triangles) and chemical vapour deposition (green circles) versus year. Although nanotubes longer than ~1 cm could conceivably be produced, the chambers of scanning electron microscopes are not large enough to characterize such long nanotubes. Ropes and yarns of much longer lengths have since been made. Figure reproduced with permission from ref. 78 (© 2007 World Scientific).

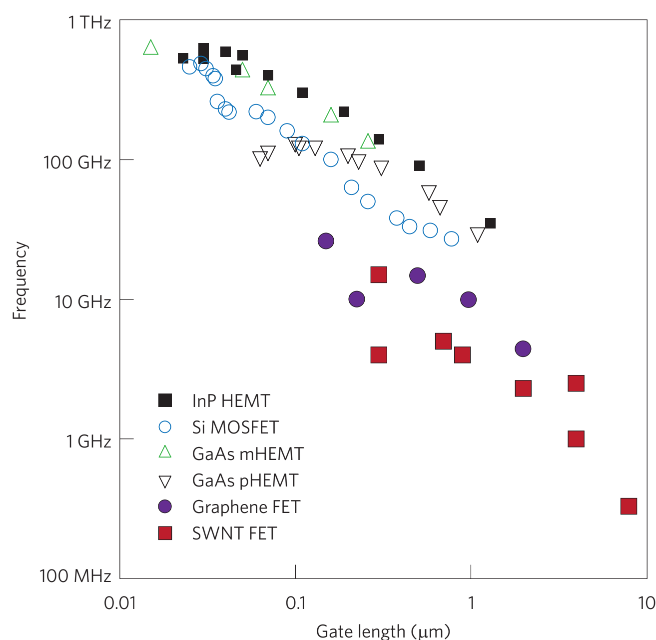



**Figure 4 | Frequency performance of different materials.** State-of-the-art frequency performance of traditional silicon[65,80–82] devices, III–V semiconductor devices (InP high electron mobility transistor (HEMT)[65], GaAs metamorphic-HEMT[65,83], and GaAs pseudomorphic-HEMT[65]), nanotube-based FETs[63,68,75,76] and graphene FETs[84–86,115] versus gate length. Data points for the nanotube-based FETs are the 'extrinsic' cut-off frequency. Silicon and III–V semiconductor data courtesy of Frank Schwierz.

The evaporating-droplet method has been successful in achieving self-assembled bands of high-density (~10–20 nanotubes $\mu m^{-1}$) aligned (within 5° of one another) nanotubes[52] (Fig. 1d). Similarly, using polar and nonpolar features patterned onto the substrate, linear droplet lines were formed and controlled nanotube deposition was achieved[53]. Although the process is conceivably scalable, the formation of periodic bands of aligned nanotubes could limit its utility for certain applications[52,53].

Table 1 summarizes the properties required of the final nanotube array for analogue RF electronics applications. Many of the techniques reviewed above can meet one or more of these metrics, such as diameters in the range 1.5–2 nm (required for high current[54,55]), but no single technique can meet all of them. Therefore, it is likely that some combination of the techniques will be required to meet the final requirements for practical device performance, which we discuss next.

## Impact of array density on RF device performance

In the small-signal limit, the a.c. performance of RF transistors can be represented by a linear circuit model consisting of a voltage-dependent current source (the transconductance) plus associated resistances and capacitances (Fig. 2b). Such a model completely describes the input and output impedances, the voltage gain and the current gain, all of which depend on frequency.

Two different definitions of gain are widely used to characterize the frequency response of the transistor[56]: the current gain $H_{21}$ is defined as the output current divided by the input current, and Mason's unilateral gain $U$ is the power gain realized under conjugate impedance-matching at the input and output when the transistor is unilateralized (that is, embedded in a feedback network to isolate the output from the input) using a lossless reciprocal network[57]. For bipolar transistors in the low-frequency limit, $H_{21}$ is better known as $\beta$, and can intuitively be considered as the current gain. For FET devices, the current gain is less intuitive, and the cut-off or transition frequency $f_T$ — the frequency at which $H_{21}$ falls to unity (0 dB) — is the most commonly quoted figure of merit, and is defined as such for both bipolar and FET technology. A more useful number for FETs is the maximum frequency of oscillation $f_{max}$, which is the frequency at which $U$ drops to unity.

Using the effective RF circuit model shown in Fig. 2b, we can express the cut-off frequency of a nanotube FET as:

$$f_T = \frac{g_m}{2\pi} \frac{1}{(C_{gs} + C_{p,gs} + C_{p,gd})((R_{p,s} + R_{p,d})g_d + 1) + C_{p,gd} g_m (R_{p,s} + R_{p,d})} \tag{1}$$

where $g_m$ is the transconductance, $g_d$ is the drain conductance, $C_{gs}$ is the gate capacitance, $C_{p,gd}$ and $C_{p,gs}$ are the parasitic gate-drain and gate-source capacitances, and $R_{p,s}$ and $R_{p,d}$ are the parasitic series resistance for the source and drain[58]. This is sometimes referred to as the extrinsic cut-off frequency to differentiate it from the intrinsic cut-off frequency (the calculated cut-off frequency when parasitics



© 2009 Macmillan Publishers Limited. All rights reserved

are ignored). Sometimes, it is numerically justifiable to ignore the effects of parasitic circuit elements, but with nanotube-based FETs they are usually significant at all frequencies. Thus, the intrinsic cut-off frequency is given by:

$$f_{\mathrm{T,intrinsic}} = \frac{g_\mathrm{m}}{2\pi C_\mathrm{gs}}$$

The intrinsic cut-off frequency can be considered the ultimate frequency performance of the device when it is not slowed down by external circuit elements. As $R_{\mathrm{p,s}}$ and $R_{\mathrm{p,d}}$ are usually external metal electrodes, they can often be made smaller with modest effort. The value of $g_\mathrm{d}$ would ideally be zero, but in the presence of metallic nanotubes, it can be significant. However, the most important extrinsic element is the parasitic capacitance. For an individual nanotube-based FET, the parasitic capacitance $C_{\mathrm{p,gs}}$ is typically about two orders of magnitude larger than the intrinsic capacitance $C_\mathrm{gs}$. (Typically, the values of both $C_{\mathrm{p,gs}}$ and $C_{\mathrm{p,gd}}$ are $\sim10^{-16}$ F μm$^{-1}$ of the gate width, whereas the $C_\mathrm{gs}$ of an individual nanotube is $\sim10^{-17}$ F μm$^{-1}$ of the nanotube length.) This reduces the cut-off frequency of individual nanotube-based FETs by about two orders of magnitude below its intrinsic limit[6,7,59–61].

To achieve the ultimate (intrinsic) limit, one must use very dense, parallel arrays of nanotubes because this increases $g_\mathrm{m}$ and $C_\mathrm{gs}$ while keeping the parasitic capacitance approximately constant. The need to use arrays to achieve the best possible performance is the most important conclusion of this Review Article.

To improve the frequency performance it is important to understand how the intrinsic cut-off frequency scales with gate length $L_\mathrm{gate}$. First, as $C_\mathrm{gs}$ is proportional to the gate area, $C_\mathrm{gs}$ for a nanotube is proportional to $L_\mathrm{gate}$. At present, it is not known how $g_\mathrm{m}$ for a nanotube scales with $L_\mathrm{gate}$, so we use classical FET theory as a guide. If $L_\mathrm{gate}$ is long, the electric field $E$ will be small (because $E = V_\mathrm{ds}/L_\mathrm{gate}$, where $V_\mathrm{ds}$ is the drain–source voltage), and the electron drift velocity will be given by $v_\mathrm{drift} = \mu E$, where $\mu$ is the mobility. On the other hand, if $L_\mathrm{gate}$ is short, then $E$ will be large, and $v_\mathrm{drift}$ will saturate at a value denoted by $v_\mathrm{sat}$. Knowing $v_\mathrm{drift}$ we can calculate the transconductance and then the cut-off frequency in these two limits by using the following expression for the drain–source current $I_\mathrm{ds} = v_\mathrm{drift}ne$, where $e$ is the charge of an individual electron, and the charge density $n = (C_\mathrm{gs}/2eL_\mathrm{gate})(V_\mathrm{gs} - V_\mathrm{T})$, where $V_\mathrm{gs}$ is the gate–source voltage, and the threshold voltage $V_\mathrm{T}$ is related to the gate– and drain–source voltages by the expression $V_\mathrm{ds} = (V_\mathrm{gs} - V_\mathrm{T})$ in the current-saturation regime. For long gates and small electric fields we find the transconductance to be $\mu C_\mathrm{gs}(V_\mathrm{gs} - V_\mathrm{T})/L_\mathrm{gate}^2$; for short gates and large electric fields it is given by $v_\mathrm{sat}(C_\mathrm{gs}/L_\mathrm{gate})$. Consequently, the cut-off frequency can be represented by two limits:

$$f_{\mathrm{T,intrinsic}} \approx \begin{cases} \mu(V_\mathrm{gate} - V_\mathrm{T}) \big/ 2\pi L_\mathrm{gate}^2 & L_\mathrm{gate}\ \text{large} \\ \dfrac{v_\mathrm{sat}}{2\pi L_\mathrm{gate}} & L_\mathrm{gate}\ \text{small} \end{cases}$$

The question of the definition of 'large' versus 'small' depends on the details of the velocity-field curve for carbon nanotubes, which is difficult to measure. Still, it is generally accepted that GHz frequency operation will involve going into the short-gate-length regime, so the mobility will not be the appropriate figure of merit to determine the response time of the transistor. In nanotubes the value of $v_\mathrm{sat}$ is estimated to be $\approx 1.2$–$2\times10^7$ cm s$^{-1}$ (based on carefully modelling both the d.c.[62] and RF[63] performance). Using these values, the predicted 'intrinsic' cut-off frequency will be ≈ 20–30 GHz/$L_\mathrm{gate}$ (μm) (depending on the value of $v_\mathrm{sat}$ assumed), which is comparable to the best III–V semiconductors.

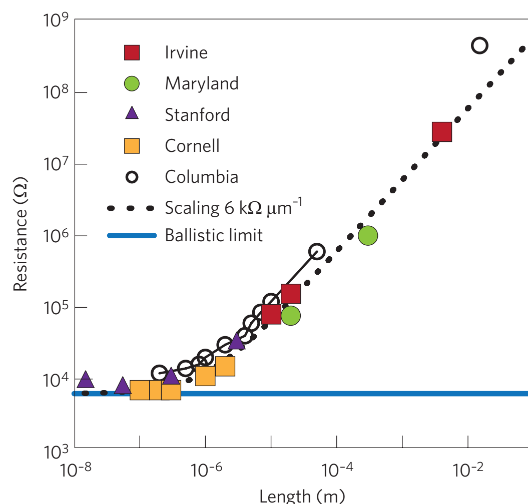



**Figure 5 | Resistance performance.** Resistance versus length for individual single-walled nanotubes at room temperature (except for the data point at 76 kΩ, 20 μm (left-most green circle), which was measured at 4.2 K; ref. 62) from various labs around the world. The Cornell University data[90] were taken by using an atomic force microscope to measure the voltage drop on an individual nanotube, whereas the Columbia University data[91,92] were taken with multiple contacts on an individual nanotube. The data points from University of California, Irvine[88,89], University of Maryland, College Park[4,62] and Stanford University[93–95] are for distinct nanotubes. All the data are consistent with single-walled nanotubes having a resistance of about 6 kΩ μm$^{-1}$ (dotted line). The ballistic limit (solid blue line) is the lowest contact resistance allowed by quantum mechanics. Reproduced with permission from ref. 87 (© 2009 Wiley).

On the other hand, for long-channel devices (such as printed electronic devices with channel lengths that are longer than 10 μm), the effective mobility determines the cut-off frequency, and here individual nanotubes also have mobilities comparable to the best III–V semiconductors. So far, nanotube-array devices that realize this intrinsic limit have not yet been demonstrated, owing to limitations from parasitic capacitances (see below), but with dense enough arrays, it should be possible to approach this intrinsic speed limit.

In the extreme short-channel limit (where transport is ballistic from source to drain), it has been argued that the carrier-injection velocity into the channel strongly influences the cut-off frequency, so the mobility also becomes important in this limit[64]. Moreover, we should note that the above arguments apply mainly to 'ideal' structures where short-channel effects, parasitic effects and the overall design (for example, metal oxide field-effect transistor (MOSFET) versus high electron mobility transistor (HEMT)) are not important, so they provide only a qualitative guide in the extreme short-channel limit. (See ref. 65 for more details).

How does one construct a thin-film transistor (TFT) that achieves the intrinsic limit discussed above? In general, the best approach is to reduce the relative importance of the parasitic capacitances (which are mainly due to the fringe fields from the electrodes, and depend only mildly on the device geometry). Thus, by increasing the number of nanotubes per width, one increases the transconductance $g_\mathrm{m}$ without a significant increase in the parasitic capacitance, allowing the ultimate limit to be reached. In this context, it is important to quantify the relationship between the cut-off frequency and the intrinsic cut-off frequency as a function of nanotube array density.

In the limit of sparse nanotube arrays (that is, when the pitch (or spacing) between the nanotubes $d$ is larger than gate–tube



© 2009 Macmillan Publishers Limited. All rights reserved

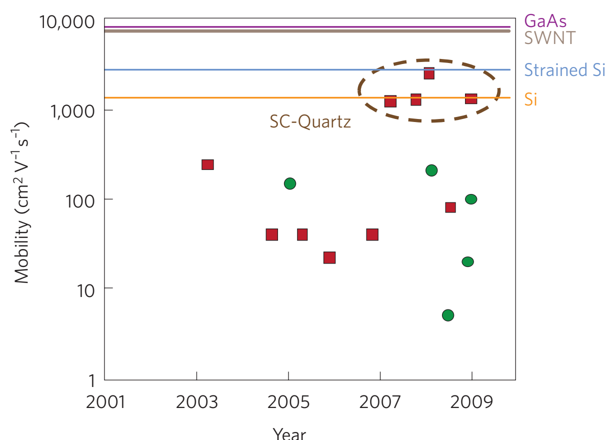



**Figure 6 | Mobility performance.** For long-channel devices, the mobility is important in achieving a large transconductance and a high cut-off frequency. This plot shows mobility versus year for TFTs made by two methods: devices made from single-walled nanotubes grown by CVD are shown as red squares[35,76,96-103], and devices made from nanotubes deposited from solution are shown as green circles (refs 51,52,104,105 and M. Ishida, S. Toguchi, H. Hongo and F. Nihet, unpublished observation). TFTs grown by CVD on single-crystal quartz substrates (red squares inside dashed line) have the highest mobilities. As a comparison, mobility values for n-type (undoped) silicon, strained silicon, an individual single-walled nanotube (diameter ~2 nm) and gallium arsenide are also shown.

separation), and neglecting $R_{p,s}$ and $R_{p,d}$ in equation (1), the cut-off frequency[7] in the presence of parasitic capacitances can be written as:

$$f_T = f_{T,\text{intrinsic}}\left(\frac{1}{1+\dfrac{C_w}{C_{gs,1}}d}\right) \qquad (2)$$

where $C_{gs,1}$ is the nanotube–gate capacitance of an individual nanotube, and $C_w$ is the parasitic capacitance per gate width defined as $(C_{p,gd} + C_{p,gs})/W$, where $W$ is the gate width (see Fig. 2). Typically[6], $C_w$ is ~$10^{-16}$ F μm$^{-1}$ and $C_{gs,1} \approx 10^{-17}$ F × $L_{gate}$ (μm) so that, ideally, one wants the spacing between the nanotubes to be less than 0.1 μm (that is, a density of 10 nanotubes μm$^{-1}$ or higher), for the cut-off frequency not to be significantly degraded by the external (parasitic) capacitance. This is achievable using some of the deposition methods described above.

Although the nanotube density is the critical parameter, $g_d$, $R_{p,s}$, and $R_{p,d}$ can cause further degradation in $f_T$ as seen in equation (1). At even higher densities, screening by adjacent nanotubes will effect the values (per nanotube) of the transconductance and gate capacitance[35,66]. However, these effects cancel in the calculation of the cut-off frequency, so equation (2) is still valid in the presence of screening, but the value of $C_{gs,1}$ will be reduced compared with the sparse case.

For RF applications, power gain is the important figure of merit (rather than current gain), so $f_{max}$ is also an important parameter. A typical approximation for $f_{max}$ is (see ref. 58):

$$f_{max} \approx \frac{f_T}{2(g_d(R_{p,s} + R_{gate}) + 2\pi f_T C_{p,gd} R_{gate})^{\frac{1}{2}}}$$

where $R_{gate}$ is the gate resistance. The value of $f_{max}$ can be made as high as possible by increasing the density of the nanotubes in the array to make $C_{p,gd}$ as small as possible. However, the presence of metallic nanotubes in the array will lead to a non-zero value of $g_d$, which will reduce $f_{max}$, and this is one of the reasons for removing the metallic nanotubes. A comprehensive study of the effects of both $R_{gate}$ and the presence of metallic nanotubes on $f_{max}$ is an important next step in the development of RF devices[67].

Although $f_T$ and $f_{max}$ are generally of the same order of magnitude, either one can be higher than the other depending on the device characteristics (see, for example, Fig. 14 in ref. 65). This is especially important for nanotube transistors, where $f_T$ can be an order of magnitude higher than $f_{max}$ (ref. 68). Thus, both $f_T$ and $f_{max}$ should be compared when comparing the performance of different nanotube transistors.

## Devices and measurements

Frequency performance has improved in the past few years, with individual nanotube-based FETs reaching frequencies up to 52 MHz in a multistage ring-oscillator[69–71], and arrays of nanotubes showing cut-off frequencies of up to ~10 GHz (refs 35,60,63,68,72–77; see Fig. 3a). The maximum length of nanotubes has also increased[78] (Fig. 3b). The next challenge on the road to higher frequencies is to increase the nanotube density and the percentage of semiconducting nanotubes.

The highest frequencies reported so far have been for nanotube devices made from samples with about two-thirds semiconducting nanotubes and densities of 5 nanotubes μm$^{-1}$ grown by CVD on quartz[63,76], or from samples that are mostly (90–95%) metallic but have been deposited at higher densities with dielectrophoresis[68,75]. Both device families achieve cut-off frequencies of ~10 GHz with gate lengths ~0.3 μm, indicating that if the fraction of semiconducting nanotubes or density can be improved, the cut-off frequency can be substantially increased. This should be possible by starting with the samples of purified semiconducting nanotubes that have recently become available in a number of labs (see, for example, refs 68 and 79).

To compare nanotubes with other materials, we plot the cut-off frequency versus gate length for nanotubes, graphene and various semiconductors in Fig. 4 (see refs 63,65,68,75,76,80–86). Although it is often assumed that high-mobility materials are needed to make high-speed FETs, this relationship generally only holds true for devices with long channels, as discussed above. For example, for submicrometre gate lengths, the speed advantages of III–V semiconductors such as GaAs and InP over Si-MOSFETs[65] are mainly due to higher saturation velocities. Graphene-based FETs use two-dimensional sheets of carbon atoms as the channel material (as opposed to the one-dimensional tubes of carbon atoms used in nanotube-based FETs), and a recent report of an extrinsic cut-off frequency of ~26 GHz for a 150-nm-gate-length device is on a par with the performance of the best nanotube-based FETs if we allow for the difference in gate length[85] (Fig. 4). However, as described above, the use of denser arrays will lead to increases in the cut-off frequency for nanotube FETs.

In contrast to submicrometre devices, the effective mobility is an important figure-of-merit for TFT devices with long channel lengths. It is generally agreed[3] that electron–phonon scattering limits the peak mobility of an individual nanotube to between 6,000 and 10,000 cm$^2$ V$^{-1}$ s$^{-1}$, with the resistance being about 6 kΩ μm$^{-1}$ (Fig. 5 and refs 87–95). The mean free-path inferred from these measurements (at low electric fields) is ~1 μm. For arrays or thin films of nanotubes, the effective mobility is related to the nanotube density, alignment and fraction of semiconducting nanotubes[5]. It is generally believed that a thin film of nanotubes, suitably prepared, should be able to achieve an 'effective' mobility comparable to that of a single nanotube level, but this has not been demonstrated yet.

In Fig. 6, we plot the mobility versus year for nanotube films prepared by the two methods discussed earlier — grow in place with CVD, and deposition from solution — along with the mobility of



© 2009 Macmillan Publishers Limited. All rights reserved

a pristine nanotube and the mobilities reported for other materials (refs 35,51,52,76,96–105 and M. Ishida, S. Toguchi, H. Hongo and F. Nihet, unpublished observation). We plot mobility values computed using $\mu = (l/WC_{gs})(1/V_{ds})\partial I_{ds}/\partial V_{gs}$ from data measured typically in the linear regime (low $V_{ds}$). However, devices typically operate in the saturation regime (high $V_{ds}$), so the mobility numbers quoted in the literature (typically measured at low $V_{ds}$) are not always a good guide to device performance.

The mobilities of randomly aligned mats of nanotubes grown in place on silicon and those deposited from solution are comparable, with wide scatter due to differences in the nanotube density, average length and, possibly, other parameters. It is generally found that the mobility (which should be independent of gate length for single nanotubes) increases with increasing gate length, even for nanotube films of nominally the same quality. Generally speaking, we still do not have a reliable method for predicting the final device mobility based on the detailed preparation parameters. However, the mobility of nanotube arrays grown by CVD on quartz[35,76,101,102] are much higher than those deposited from solution onto other substrates.

Nanotubes deposited from solution have much higher mobilities than organic semiconductors (which typically have mobilities of ~1 $cm^2 V^{-1} s^{-1}$; ref. 106), and therefore they could compete with organics in applications that require only moderate mobilities such as low-cost printed electronic circuits. Although techniques for making printed circuits typically achieve resolutions (and hence gate lengths) of ~10 μm, the recent introduction of self-aligned techniques to the manufacture of printed circuits has allowed submicrometre gate lengths to be achieved, even in inkjet printed devices[107]. This approach has been shown to minimize the overlap parasitic capacitance and has made it possible to achieve a cut-off frequency 1.6 MHz from a starting material with a mobility of ~0.2 $cm^2 V^{-1} s^{-1}$ and a gate length of 200 nm. If this new self-aligned approach to making printed electronics could be combined with the nanotube TFTs made with the solution-based approach (which have mobilities up to about 200 $cm^2 V^{-1} s^{-1}$; M. Ishida, S. Toguchi, H. Hongo and F. Nihet, unpublished observation), it might be possible (neglecting velocity saturation effects discussed above) to increase the cut-off frequency by a factor of 1,000 to give $f_T > 1$ GHz. Such an accomplishment would represent a great leap forward on the road to high-frequency low-cost circuit applications such as all-printed RF identification tags[108].

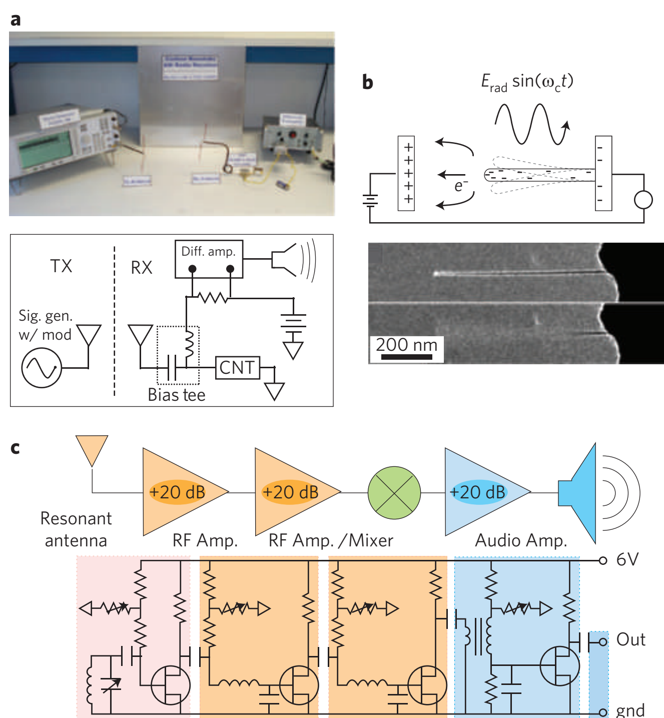



**Figure 7 | Nanotubes are performing increasingly complex roles in AM radios. a**, A nanotube (CNT) acts as a RF detector in an AM radio. The other components in this demonstration include a signal generator, which is used to transmit (TX) wirelessly an amplitude-modulated signal (sig. gen. w/mod) to the receiver (RX), which consists of a bias tee, a differential amplifier (diff. amp.), a speaker and battery. Reproduced with permission from ref. 109 (© 2007 ACS). **b**, A nanotube in high vacuum acts as a RF detector and an integrated RF filter in an AM radio, where an oscillating electric field ($E_{rad}\sin(\omega_c t)$) induces the vibration of the tube. Reproduced with permission from ref. 110 (© 2007 ACS). **c**, Nanotube-based FETs act as the RF pre-amplifier, detector (mixer) and audio-frequency amplifier, thus demonstrating a complete AM radio system. Reproduced with permission from ref. 76 (© 2008 PNAS).

## Demonstrations of nanotubes in RF applications

Recently, several groups have gone beyond device characterization and demonstrated applications in actual radio systems. Although these radios are not yet commercially competitive with existing systems, it is an important milestone to be able to demonstrate operating systems.

Our lab at the University of California, Irivne[109] and another lab at the University of California, Berkeley[110] have used a nanotube as the demodulator in a radio receiver, and have demonstrated a functioning radio that can pick up a signal generated in the lab by a separate generator and play music broadcast wirelessly across a room. Since the demodulation occurs owing to the nonlinearity in the source–drain current–voltage characteristics, it does not matter whether a metallic or semiconducting nanotube is used in this case. The nanotube itself simply detected an amplitude-modulated (AM) signal (replacing the diode in a classical AM radio) and, as such, does not present any particular advantage, other than small size. Moreover, the overall radio system is still large because the external components (the antenna, battery, audio amplifier and so on) are still large (Fig. 7). The UC Berkeley work adds further functionality by using the mechanical resonance frequency of the nanotube as an integrated RF filter, an elegant step towards an integrated nanoradio, but at the cost of requiring a high vacuum. Furthermore, neither of these radios were sensitive enough to receive weak radio signals from local radio stations due to lack of an RF pre-amplifier at the front end.

A recent collaboration between the University of Illinois at Urbana-Champaign and Northrop Grumman has demonstrated the first RF amplifier based on a nanotube FET, and used it in an entire AM radio system[76]. Separate nanotube transistors also functioned as the RF detector (actually mixer) and audio amplifier. Because an RF pre-amplifier was used, the radio was able to receive weak signals from a local radio station. This demonstrates the application of nanotube electronics into a fully functional system.

Although these demonstrations show that it is possible to make nanoscale components, a true nanoradio would require all the components — including the power source (battery), antenna and the signal-processing elements — to be nanoscale. Using the RF field itself as a power source would completely obviate the need for the battery, while the use of on-chip antennas[111] or even nano-antennas[112,113] would allow for much smaller radios. More research is needed to address the trade-offs between efficiency, required external power, antenna size and heating. Based on standard CMOS technology, we have argued that a single-chip radio system (including antenna and providing space for on-board sensors) of size 100 × 100 × 1 μm is feasible, which begins to approach the size of a single living cell[114]. A true nanoradio should eventually be possible with further developments in nanotechnology.



© 2009 Macmillan Publishers Limited. All rights reserved

## Summary

To obtain high-performance nanotube-based RF-FETs, dense aligned arrays of all-semiconducting nanotubes are required. Progress in this direction has been rapid, and there are several potential routes towards manufacturing such materials. The advantages of high linearity predicted for one-dimensional materials, together with relaxed manufacturing tolerances, may be the defining advantage over other materials for analogue RF devices. Initial systems have been demonstrated by multiple research labs, and if the previous rate of progress is any indication, it is entirely feasible that, rather than extending Moore's law for digital electronics, the initial point of insertion of nanotube technology into commercial electronics markets will be in wireless communications systems of various kinds.


## References


1. Dresselhaus, M. S., Dresselhaus, G. & Eklund, P. C. *Science of Fullerenes and Carbon Nanotubes*. (Academic Press, 1996).
2. Saito, R., Dresselhaus, G. & Dresselhaus, M. S. *Physical Properties of Carbon Nanotubes*. (Imperial College Press, 1998).
3. Zhou, X. J., Park, J. Y., Huang, S. M., Liu, J. & McEuen, P. L. Band structure, phonon scattering, and the performance limit of single-walled carbon nanotube transistors. *Phys. Rev. Lett.* **95,** 146805 (2005).
4. Durkop, T., Getty, S. A., Cobas, E. & Fuhrer, M. S. Extraordinary mobility in semiconducting carbon nanotubes. *Nano Lett.* **4,** 35–39 (2004).
5. Cao, Q. & Rogers, J. Ultrathin films of single-walled carbon nanotubes for electronics and sensors: A review of fundamental and applied aspects. *Adv. Mater.* **21,** 29–53 (2009).
6. Burke, P. J. AC performance of nanoelectronics: Towards a ballistic THz nanotube transistor. *Solid State Electron.* **40,** 1981–1986 (2004).
7. Guo, J., Hasan, S., Javey, A., Bosman, G. & Lundstrom, M. Assessment of high-frequency performance potential of carbon nanotube transistors. *IEEE Trans. Nanotech.* **4,** 715–721 (2005).
8. Alam, K. & Lake, R. Performance of 2 nm gate length carbon nanotube field-effect transistors with source/drain underlaps. *Appl. Phys. Lett.* **87,** 073104 (2005).
9. Hasan, S., Salahuddin, S., Vaidyanathan, M. & Alam, A. A. High-frequency performance projections for ballistic carbon-nanotube transistors. *IEEE Trans. Nanotech.* **5,** 14–22 (2006).
10. Castro, L. C. *et al.* Method for predicting $f_T$ for carbon nanotube FETs. *IEEE Trans. Nanotech.* **4,** 699–704 (2005).
11. Yoon, Y., Ouyang, Y. & Guo, J. Effect of phonon scattering on intrinsic delay and cutoff frequency of carbon nanotube FETs. *IEEE Trans. Electron Dev.* **53,** 2467–2470 (2006).
12. Baumgardner, J. E. *et al.* Inherent linearity in carbon nanotube field-effect transistors. *Appl. Phys. Lett.* **91,** 052107 (2007).
13. Ural, A., Li, Y. M. & Dai, H. J. Electric-field-aligned growth of single-walled carbon nanotubes on surfaces. *Appl. Phys. Lett.* **81,** 3464–3466 (2002).
14. Joselevich, E. & Lieber, C. M. Vectorial growth of metallic and semiconducting single-wall carbon nanotubes. *Nano Lett.* **2,** 1137–1141 (2002).
15. Huang, S. M., Cai, X. Y. & Liu, J. Growth of millimeter-long and horizontally aligned single-walled carbon nanotubes on flat substrates. *J. Am. Chem. Soc.* **125,** 5636–5637 (2003).
16. Huang, S., Woodson, M., Smalley, R. & Liu, J. Growth mechanism of oriented long single walled carbon nanotubes using fast-heating chemical vapor deposition process. *Nano Lett.* **4,** 1025–1028 (2004).
17. Yu, Z., Li, S. & Burke, P. J. Synthesis of aligned arrays of millimeter long, straight single walled carbon nanotubes. *Chem. Mater.* **16,** 3414–3416 (2004).
18. Huang, L. *et al.* Cobalt ultrathin film catalyzed ethanol chemical vapor deposition of single-walled carbon nanotubes. *J. Phys. Chem. B* **110,** 11103–11109 (2006).
19. Ismach, A., Segev, L., Wachtel, E. & Joselevich, E. Atomic-step-templated formation of single wall carbon nanotube patterns. *Angew. Chem. Int. Ed.* **43,** 6140–6143 (2004).
20. Ago, H. *et al.* Aligned growth of isolated single-walled carbon nanotubes programmed by atomic arrangement of substrate surface. *Chem. Phys. Lett.* **408,** 433–438 (2005).
21. Han, S., Liu, X. L. & Zhou, C. W. Template-free directional growth of single-walled carbon nanotubes on a- and r-plane sapphire. *J. Am. Chem. Soc.* **127,** 5294–5295 (2005).
22. Kocabas, C. *et al.* Guided growth of large-scale, horizontally aligned arrays of single-walled carbon nanotubes and their use in thin-film transistors. *Small* **1,** 1110–1116 (2005).
23. Ago, H. *et al.* Competition and cooperation between lattice-oriented growth and step-templated growth of aligned carbon nanotubes on sapphire. *Appl. Phys. Lett.* **90,** 123112 (2007).
24. Ding, L., Yuan, D. N. & Liu, J. Growth of high-density parallel arrays of long single-walled carbon nanotubes on quartz substrates. *J. Am. Chem. Soc.* **130,** 5428–5429 (2008).
25. Zhou, W. W., Rutherglen, C. & Burke, P. Wafer scale synthesis of dense aligned arrays of single-walled carbon nanotubes. *Nano Research* **1,** 158–165 (2008).
26. Kang, S. J. *et al.* Printed multilayer superstructures of aligned single-walled carbon nanotubes for electronic, applications. *Nano Lett.* **7,** 3343–3348 (2007).
27. Zhang, G. *et al.* Selective etching of metallic carbon nanotubes by gas-phase reaction. *Science* **314,** 974–977 (2006).
28. Yang, C. M. *et al.* Preferential etching of metallic single-walled carbon nanotubes with small diameter by fluorine gas. *Phys. Rev. B.* **73,** 075419 (2006).
29. Ding, L. *et al.* Selective growth of well-aligned semiconducting single-walled carbon nanotubes. *Nano Lett.* **9,** 800–805 (2009).
30. Li, Y. *et al.* Preferential growth of semiconducting single-walled carbon nanotubes by a plasma enhanced CVD method. *Nano Lett.* **4,** 317–321 (2004).
31. An, L., Fu, Q., Lu, C. & Liu, J. A simple chemical route to selectively eliminate metallic carbon nanotubes in nanotube network devices. *J. Am. Chem. Soc.* **126,** 10520–10521 (2004).
32. Balasubramanian, K., Sordan, R., Burghard, M. & Kern, K. A selective electrochemical approach to carbon nanotube field-effect transistors. *Nano Lett.* **4,** 827–830 (2004).
33. Strano, M. S. *et al.* Electronic structure control of single-walled carbon nanotube functionalization. *Science* **301,** 1519–1522 (2003).
34. Collins, P. C., Arnold, M. S. & Avouris, P. Engineering carbon nanotubes and nanotube circuits using electrical breakdown. *Science* **292,** 706–709 (2001).
35. Kang, S. J. *et al.* High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes. *Nature Nanotech.* **2,** 230–236 (2007).
36. Amlani, I. *et al.* in *8th IEEE Conf. Nanotech* 239–242 (IEEE, 2008).
37. Lin, A. *et al.* Threshold voltage and on-off ratio tuning for multiple-tube carbon nanotube FETs. *IEEE Trans. Nanotech.* **8,** 4–9 (2009).
38. Ryu, K. *et al.* CMOS-analogous wafer-scale nanotube-on-insulator approach for submicrometer devices and integrated circuits using aligned nanotubes. *Nano Lett.* **9,** 189–197 (2009).
39. Shim, H., Song, J., Kwak, Y., Kim, S. & Han, C. Preferential elimination of metallic single-walled carbon nanotubes using microwave irradiation. *Nanotechnology* **20,** 065707 (2009).
40. Huang, H., Maruyama, R., Noda, K., Kajiura, H. & Kadono, K. Preferential destruction of metallic single-walled carbon nanotubes by laser irradiation. *J. Phys. Chem. B* **110,** 7316–7320 (2006).
41. Hersam, M. Progress towards monodisperse single-walled carbon nanotubes. *Nature Nanotech.* **3,** 387–394 (2008).
42. Li, X. *et al.* Langmuir-Blodgett assembly of densely aligned single-walled carbon nanotubes from bulk materials. *J. Am. Chem. Soc.* **129,** 4890–4891 (2007).
43. Rutherglen, C., Jain, D. & Burke, P. RF resistance and inductance of massively parallel single walled carbon nanotubes: Direct, broadband measurements and near perfect 50 ohm impedance matching. *Appl. Phys. Lett.* **93,** 083119 (2008).
44. Krupke, R., Linden, S., Rapp, M. & Hennrich, F. Thin films of metallic carbon nanotubes prepared by dielectrophoresis. *Adv. Mater.* **18,** 1468–1468 (2006).
45. Boccaccini, A. R. *et al.* Electrophoretic deposition of carbon nanotubes. *Carbon* **44,** 3149–3160 (2006).
46. Morgan, H. & Green, N. G. *AC Electrokinetics: Colloids and Nanoparticles* (Research Studies Press, 2003).
47. Krupke, R., Hennrich, F., Lohneysen, H. & Kappes, M. M. Separation of metallic from semiconducting single-walled carbon nanotubes. *Science* **301,** 344–347 (2003).
48. Krupke, R., Hennrich, F., Kappes, M. & Lohneysen, H. Surface conductance induced dielectrophoresis of semiconducting single-walled carbon nanotubes. *Nano Lett.* **4,** 1395–1400 (2004).
49. Baik, S., Usrey, M., Rotkina, L. & Strano, M. Using the selective functionalization of metallic single-walled carbon nanotubes to control dielectrophoretic mobility. *J. Phys. Chem. B* **108,** 15560–15564 (2004).
50. Kim, Y. *et al.* Dielectrophoresis of surface conductance modulated single-walled carbon nanotubes using catanionic surfactants. *J. Phys. Chem. B* **110,** 1541–1545 (2006).
51. LeMieux, M. C. *et al.* Self-sorted, aligned nanotube networks for thin-film transistors. *Science* **321,** 101–104 (2008).
52. Engel, M. *et al.* Thin film nanotube transistors based on self-assembled, aligned, semiconducting carbon nanotube arrays. *ACS Nano* **2,** 2445–2452 (2008).
53. Sharma, R., Lee, C. Y., Choi, J. H., Chen, K. & Strano, M. S. Nanometer positioning, parallel alignment, and placement of single anisotropic nanoparticles using hydrodynamic forces in cylindrical droplets. *Nano Lett.* **7,** 2693–2700 (2007).
54. Chen, Z., Appenzeller, J., Knoch, J., Lin, Y.-M. & Avouris, P. The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors. *Nano Lett.* **5,** 1497–1502 (2005).




© 2009 Macmillan Publishers Limited. All rights reserved

55. Kim, W. *et al.* Electrical contacts to carbon nanotubes down to 1 nm in diameter. *Appl. Phys. Lett.* **87,** 173101 (2005).
56. Liu, W. Fundamentals of III-V devices: HBTs, MESFETs, and HFETs/HEMTs. (Wiley, 1999).
57. Gupta, M. S. Power gain in feedback amplifiers, a classic revisited. *IEEE Trans. Microw. Theory* **40,** 864–879 (1992).
58. Schwierz, F. & Liou, J. J. *Modern Microwave Transistors: Theory, Design, and Performance.* (Wiley-Interscience, 2003).
59. Akinwande, D., Close, G. E. & Wong, H. S. P. Analysis of the frequency response of carbon nanotube transistors. *IEEE Trans. Nanotech.* **5,** 599–605 (2006).
60. Wang, D., Yu, Z., McKernan, S. & Burke, P. Ultra high frequency carbon nanotube transistor based on a single nanotube. *IEEE Trans. Nanotech.* **6,** 400–403 (2007).
61. Chaste, J. *et al.* Single carbon nanotube transistor at GHz frequency. *Nano Lett.* **8,** 525–528 (2008).
62. Chen, Y. F. & Fuhrer, M. S. Electric field-dependent charge-carrier velocity in semiconducting carbon nanotubes. *Phys. Rev. Lett.* **95,** 236803 (2005).
63. Kocabas, C. *et al.* High-frequency performance of submicrometer transistors that use aligned arrays of single-walled carbon nanotubes. *Nano Lett.* **8,** 1937–1943 (2009).
64. Lundstrom, M. Elementary scattering theory of the Si MOSFET. *IEEE Electr. Device Lett.* **18,** 361–363 (1997).
65. Schwierz, F. & Liou, J. J. RF transistors: Recent developments and roadmap toward terahertz applications. *Solid State Electron.* **51,** 1079–1091 (2007).
66. Cao, Q. *et al.* Gate capacitance coupling of singled-walled carbon nanotube thin-film transistors. *Appl. Phys. Lett.* **90,** 023516 (2007).
67. Castro, L. C. & Pulfrey, D. L. Extrapolated $f_{max}$ for carbon nanotube field-effect transistors. *Nanotechnology* **17,** 300–304 (2006).
68. Nougaret, L. *et al.* 80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes. *Appl. Phys. Lett.* **94,** 243505 (2009).
69. Bachtold, A., Hadley, P., Nakanishi, T. & Dekker, C. Logic circuits with carbon nanotube transistors. *Science* **294,** 1317–1320 (2001).
70. Javey, A., Wang, Q., Ural, A., Li, Y. M. & Dai, H. J. Carbon nanotube transistor arrays for multistage complementary logic and ring oscillators. *Nano Lett.* **2,** 929–932 (2002).
71. Chen, Z. H. *et al.* An integrated logic circuit assembled on a single carbon nanotube. *Science* **311,** 1735–1735 (2006).
72. Narita, K., Hongo, H., Ishida, M. & Nihey, F. High-frequency performance of multiple-channel carbon nanotube transistors. *Phys. Status Solidi A* **204,** 1808–1813 (2007).
73. Bethoux, J. M. *et al.* Active properties of carbon nanotube field-effect transistors deduced from S parameters measurements. *IEEE Trans. Nanotech.* **5,** 336–342 (2006).
74. Bethoux, J. M. *et al.* An 8-GHz $f_T$ carbon nanotube field-effect transistor for gigahertz range applications. *IEEE Electron Dev. Lett.* **27,** 681–683 (2006).
75. Louarn, A. L. *et al.* Intrinsic current gain cutoff frequency of 30 GHz with carbon nanotube transistors. *Appl. Phys. Lett.* **90,** 233108 (2007).
76. Kocabas, C. *et al.* Radio frequency analog electronics based on carbon nanotube transistors. *Proc. Natl Acad. Sci. USA* **105,** 1405–1409 (2008).
77. Chimot, N. *et al.* Gigahertz frequency flexible carbon nanotube transistors. *Appl. Phys. Lett.* **91,** 153111 (2007).
78. Burke, P. J. *Nanotubes and Nanowires* (World Scientific, 2007).
79. Rutherglen, C. *Carbon Nanotube Based Analog RF Devices* PhD thesis, Univ. California, Irvine (2009).
80. Dimitrov, V. *et al.* Small-signal performance and modeling of sub-50 nm nMOSFETs with $f_T$ above 460 GHz. *Solid State Electron.* **52,** 899–908 (2008).
81. Stork, J. in *Proc. Symp. VLSI Tech. Dig.* 1–2 (IEEE, 2006).
82. Lee, S. *et al.* in *Electron Devices Meeting IEDM* 255–258 (IEEE, 2007).
83. Yeon, S., Park, M., Choi, J. & Seo, K. in *Electron Devices Meeting IEDM* 613–616 (IEEE, 2007).
84. Moon, J. S. *et al.* Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates. *IEEE Electr. Device Lett.* **30,** 650–652 (2009).
85. Lin, Y. *et al.* Operation of graphene transistor at gigahertz frequencies. *Nano Lett.* **9,** 422–426 (2009).
86. Meric, I., Baklitskaya, P., Kim, P. & Shepard, K. RF performance of top-gated, zero-bandgap graphene field-effect transistor. *Electron Devices Meeting IEDM* 1–4 (IEEE, 2008).
87. Rutherglen, C. & Burke, P. Nanoelectromagnetics: Circuit and electromagnetic properties of carbon nanotubes. *Small* **5,** 884–906 (2009).
88. Li, S., Yu, Z., Yen, S. F., Tang, W. C. & Burke, P. J. Carbon nanotube transistor operation at 2.6 GHz. *Nano Lett.* **4,** 753–756 (2004).
89. Li, S. D., Yu, Z., Rutherglen, C. & Burke, P. J. Electrical properties of 0.4 cm long single-walled carbon nanotubes. *Nano Lett.* **4,** 2003–2007 (2004).
90. Park, J. Y. *et al.* Electron-phonon scattering in metallic single-walled carbon nanotubes. *Nano Lett.* **4,** 517–520 (2004).
91. Hong, B. H. *et al.* Quasi-continuous growth of ultralong carbon nanotube arrays. *J. Am. Chem. Soc.* **127,** 15336–15337 (2005).
92. Purewal, M. S. *et al.* Scaling of resistance and electron mean free path of single-walled carbon nanotubes. *Phys. Rev. Lett.* **98,** 186808 (2007).
93. Javey, A., Guo, J., Wang, Q., Lundstrom, M. & Dai, H. J. Ballistic carbon nanotube field-effect transistors. *Nature* **424,** 654–657 (2003).
94. Javey, A., Qi, P. F., Wang, Q. & Dai, H. J. Ten- to 50-nm-long quasi-ballistic carbon nanotube devices obtained without complex lithography. *Proc. Natl Acad. Sci. USA* **101,** 13408–13410 (2004).
95. Javey, A. *et al.* High-field quasiballistic transport in short carbon nanotubes. *Phys. Rev. Lett.* **92,** 106804 (2004).
96. Snow, E. S., Novak, J. P., Campbell, P. M. & Park, D. Random networks of carbon nanotubes as an electronic material. *Appl. Phys. Lett.* **82,** 2145–2147 (2003).
97. Zhou, Y. *et al.* P-channel, n-channel thin film transistors and p–n diodes based on single wall carbon nanotube networks. *Nano Lett.* **4,** 2031–2036 (2004).
98. Ozel, T., Gaur, A., Rogers, J. & Shim, M. Polymer electrolyte gating of carbon nanotube network transistors. *Nano Lett.* **5,** 905–911 (2005).
99. Hur, S. *et al.* Printed thin-film transistors and complementary logic gates that use polymer-coated single-walled carbon nanotube networks. *J. Appl. Phys.* **98,** 114302 (2005).
100. Cao, Q. *et al.* Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates. *Nature* **454,** 495–500 (2008).
101. Ishikawa, F. N. *et al.* Transparent electronics based on transfer printed aligned carbon nanotubes on rigid and flexible substrates. *ACS Nano* **3,** 73–79 (2009).
102. Kocabas, C., Kang, S. J., Ozel, T., Shim, M. & Rogers, J. A. Improved synthesis of aligned arrays of single-walled carbon nanotubes and their implementation in thin film type transistors. *J. Phys. Chem. C* **111,** 17879–17886 (2007).
103. Cao, Q., Xia, M., Shim, M. & Rogers, J. Bilayer organic-inorganic gate dielectrics for high-performance, low-voltage, single-walled carbon nanotube thin-film transistors, complementary logic gates, and p–n diodes on plastic substrates. *Adv. Funct. Mater.* **16,** 2355–2362 (2006).
104. Snow, E. S., Campbell, P. M., Ancona, M. G. & Novak, J. P. High-mobility carbon-nanotube thin-film transistors on a polymeric substrate. *Appl. Phys. Lett.* **86,** 033105 (2005).
105. Kanungo, M., Lu, H., Malliaras, G. & Blanchet, G. Suppression of metallic conductivity of single-walled carbon nanotubes by cycloaddition reactions. *Science* **323,** 234–237 (2009).
106. Bao, Z. & Locklin, J. J. *Organic Field-Effect Transistors* (CRC Press, 2007).
107. Noh, Y. Y., Zhao, N., Caironi, M. & Sirringhaus, H. Downscaling of self-aligned, all-printed polymer thin-film transistors. *Nature Nanotech.* **2,** 784–789 (2007).
108. Subramanian, V. *et al.* Progress toward development of all-printed RFID tags: Materials, processes, and devices. *Proc. IEEE* **93,** 1330–1338 (2005).
109. Rutherglen, C. & Burke, P. Carbon nanotube radio. *Nano Lett.* **7,** 3296–3299 (2007).
110. Jensen, K., Weldon, J., Garcia, H. & Zettl, A. Nanotube radio. *Nano Lett.* **7,** 3508–3511 (2007).
111. O, K. *et al.*, On-chip antennas in silicon ICs and their application. *IEEE Trans. Electron Dev.* **52,** 1312–1323 (2005).
112. Burke, P. J., Li, S. D. & Yu, Z. Quantitative theory of nanowire and nanotube antenna performance. *IEEE Trans. Nanotech.* **5,** 314–334 (2006).
113. Hanson, G. W. Fundamental transmitting properties of carbon nanotube antennas. *IEEE Trans. Antenn. Propag.* **53,** 3426–3435 (2005).
114. Burke, P. & Rutherglen, C. Towards a single-chip, implantable RFID system: Is a single-cell radio possible? *Biomed. Microdevices* doi:10.1007/s10544-008-9266-4 (2009).
115. Farmer, D. B. *et al.* Utilization of a buffered dielectric to achieve high field-effect carrier mobility in graphene transistors. *Nano Lett.* doi:10.1021/nl902788u (2009).



## Acknowledgements
This work was funded by the National Science Foundation, the Army Research Office, the Office of Naval Research, Northrop Grumman and the Korean National Science Foundation (KOSEF) World Class University (WCU) programme.


## Additional information
The authors declare competing financial interests: details accompany the paper at www.nature.com/naturenanotechnology.



© 2009 Macmillan Publishers Limited. All rights reserved

nature nanotechnology

REVIEW ARTICLE

PUBLISHED ONLINE: 30 MAY 2010 | DOI: 10.1038/NNANO.2010.89

# Graphene transistors

Frank Schwierz[1]*

**Graphene has changed from being the exclusive domain of condensed-matter physicists to being explored by those in the electron-device community. In particular, graphene-based transistors have developed rapidly and are now considered an option for post-silicon electronics. However, many details about the potential performance of graphene transistors in real applications remain unclear. Here I review the properties of graphene that are relevant to electron devices, discuss the trade-offs among these properties and examine their effects on the performance of graphene transistors in both logic and radiofrequency applications. I conclude that the excellent mobility of graphene may not, as is often assumed, be its most compelling feature from a device perspective. Rather, it may be the possibility of making devices with channels that are extremely thin that will allow graphene field-effect transistors to be scaled to shorter channel lengths and higher speeds without encountering the adverse short-channel effects that restrict the performance of existing devices. Outstanding challenges for graphene transistors include opening a sizeable and well-defined bandgap in graphene, making large-area graphene transistors that operate in the current-saturation regime and fabricating graphene nanoribbons with well-defined widths and clean edges.**

Every now and again, a single paper ignites a revolution in science and technology. Such a revolution was started in October 2004, when condensed-matter physicists reported that they had prepared graphene—two-dimensional sheets of carbon atoms—and observed the electric field effect in their samples[1]. It was not long before this new material attracted the attention of the electron-device community, and today a growing number of groups are successfully fabricating graphene transistors. Major chip-makers are now active in graphene research and the International Technology Roadmap for Semiconductors, the strategic planning document for the semiconductor industry, considers graphene to be among the candidate materials for post-silicon electronics[2].

Several excellent reviews on the basic science of graphene have been published in recent years[3–5]. Given the growing interest in graphene in the electron-device community, and ongoing discussions of the potential of graphene transistors, a review article focusing on graphene devices is timely. Here, from the point of view of a device engineer, I discuss the potential of graphene as a new material for electron devices, and summarize the state of the art for graphene transistors. I will focus mostly on the field-effect transistor (FET), because this is the most successful device concept in electronics and because most work on graphene devices so far has been related to FETs.

Two principal divisions of semiconductor electronics are digital logic devices and radiofrequency devices. The degree of readiness to introduce new device concepts is generally higher for radiofrequency applications, in part because the fortunes of digital logic depend almost entirely on the performance of a single type of device: the silicon metal–oxide–semiconductor FET (MOSFET). For decades, making MOSFETs smaller has been key to the progress in digital logic. This size scaling has enabled the complexity of integrated circuits to double every 18 months, leading to significant improvements in performance and decreases in price per transistor[6,7]. Today, processors containing two billion MOSFETs, many with gate lengths of just 30 nm, are in mass production (Fig. 1).

Because the fabrication of integrated circuits is highly complex, semiconductor fabrication plants are extremely expensive (at present costing several billion US dollars). Furthermore, because scaling alone has provided the needed performance improvements from one generation of integrated circuits to the next, there has been little motivation for the chip-makers to introduce devices based on a fundamentally different physics or on a material other than silicon. However, there is a consensus in the community that MOSFET scaling is approaching its limits and that, in the long run, it will be necessary to introduce new material and device concepts to ensure that performance continues to improve.

The situation is different for radiofrequency electronics. This field was dominated by defence applications until the late 1980s, and although it moved into the mainstream in the 1990s owing to advances in wireless communications, the military continued to provide generous financial support for research into new radiofrequency devices. This, together with the fact that radiofrequency circuits are much less complex than digital logic chips, has led to makers of radiofrequency chips being more open to new device concepts. An indication of this is the large variety of different transistor types and materials used in radiofrequency electronics: these include high-electron-mobility transistors (HEMTs) based on III–V semiconductors such as GaAs and InP, silicon n-channel MOSFETs, and different types of bipolar transistor[8,9].

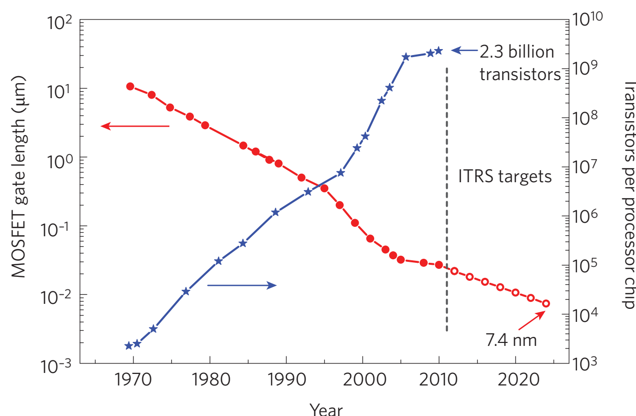



**Figure 1 | Trends in digital electronics.** Evolution of MOSFET gate length in production-stage integrated circuits (filled red circles) and International Technology Roadmap for Semiconductors (ITRS) targets (open red circles). As gate lengths have decreased, the number of transistors per processor chip has increased (blue stars). Maintaining these trends is a significant challenge for the semiconductor industry, which is why new materials such as graphene are being investigated.

[1]Technische Universität Ilmenau, Postfach 100565, 98694 Ilmenau, Germany. *e-mail: frank.schwierz@tu-ilmenau.de



© 2010 Macmillan Publishers Limited. All rights reserved

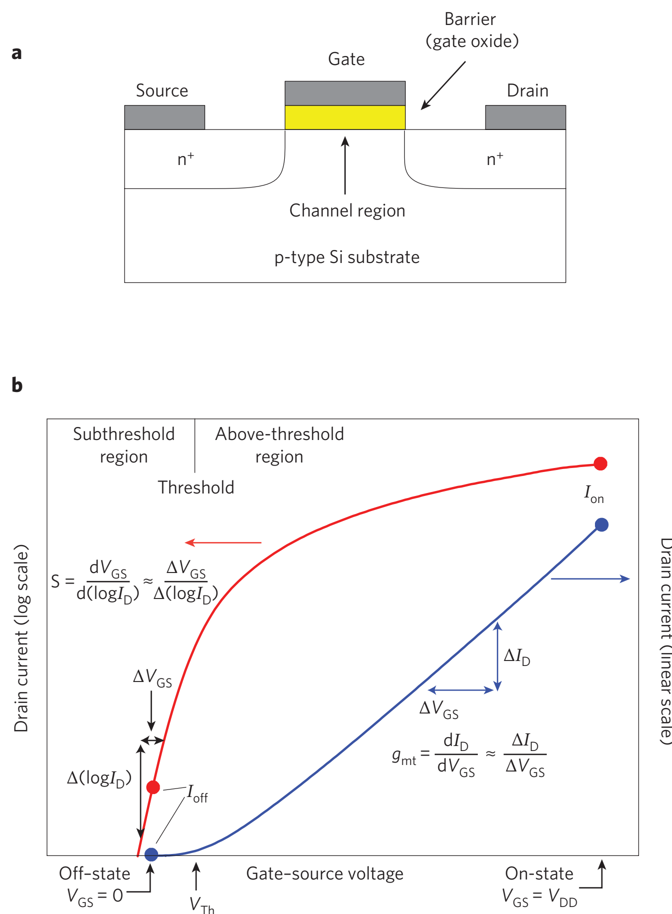



**Figure 2 | Conventional FETs. a**, Cross-section of an n-channel Si MOSFET. When the voltage applied between the source and gate electrodes exceeds a threshold voltage, $V_{Th}$, a conducting channel is formed and a drain current, $I_D$, flows. The length of the channel is defined by the length of the gate electrode; the thickness of the gate-controlled channel region is the depth to which the electronic properties of the semiconductor (p-doped Si in this case) are influenced by the gate. **b**, FET transfer characteristics showing $I_D$ (on a logarithmic scale on the left and a linear scale on the right) versus the gate–source voltage, $V_{GS}$. The transistor is considered to be switched on when $V_{GS}$ is equal to the maximum voltage supplied to the device, $V_{DD}$. The higher the slope in the subthreshold region ($V_{GS} < V_{Th}$), the better the transistor switch-on characteristics become. Above threshold, the change in $I_D$ for a given change in $V_{GS}$ is called the terminal transconductance, $g_{mt}$.

As I discuss below, graphene is potentially well suited to radiofrequency applications because of its promising carrier transport properties and its purely two-dimensional structure. This, combined with the relative openness of the radiofrequency-electronics industry to new materials, suggests that graphene might make its first appearance in radiofrequency applications rather than in logic circuits.

## FET physics: what really matters

A FET consists of a gate, a channel region connecting source and drain electrodes, and a barrier separating the gate from the channel (Fig. 2a). The operation of a conventional FET relies on the control of the channel conductivity, and thus the drain current, by a voltage, $V_{GS}$, applied between the gate and source.

For high-speed applications, FETs should respond quickly to variations in $V_{GS}$; this requires short gates and fast carriers in the channel. Unfortunately, FETs with short gates frequently suffer from degraded electrostatics and other problems (collectively known as short-channel effects), such as threshold-voltage roll-off, drain-induced barrier lowering, and impaired drain-current saturation[7,10]. Scaling theory predicts that a FET with a thin barrier and a thin gate-controlled region (measured in the vertical direction in Fig. 2a) will be robust against short-channel effects down to very short gate lengths (measured in the horizontal direction in Fig. 2a)[11]. The possibility of having channels that are just one atomic layer thick is perhaps the most attractive feature of graphene for use in transistors. (Mobility, which is often considered to be graphene's most useful property for applications in nanoelectronics, is discussed later.) By comparison, the channels in III–V HEMTs are typically 10–15 nm thick, and although silicon-on-insulator MOSFETs with channel (that is, silicon body) thicknesses of less than 2 nm have been reported[12], rough interfaces caused their mobility to deteriorate. More importantly, the body of these MOSFETs showed thickness fluctuations that will lead to unacceptably large threshold-voltage variations (and similar problems are expected to occur when the thickness of the channel in a III–V HEMT is reduced to only a few nanometres). These problems occur at thicknesses that are many times greater than the thickness of graphene.

The series resistances between the channel and the source and drain terminals are also important, and their adverse impact on the FET becomes more pronounced as the gate length decreases[13]. Thus, device engineers devote considerable effort to developing transistor designs in which short-channel effects are suppressed and series resistances are minimized.

Modern digital logic is based on silicon complementary metal oxide semiconductor (CMOS) technology. CMOS logic gates consist of both n- and p-channel MOSFETs that can switch between the on-state (with a large on-current, $I_{on}$, and $V_{GS} = \pm V_{DD}$, where $V_{DD}$ is the maximum voltage supplied to the device) and the off-state (with a small off-current, $I_{off}$, and $V_{GS} = 0$). In the terminology of digital logic, a gate is not the gate terminal of a transistor but a combination of two or more transistors that can perform a certain logic operation. The value of $V_{GS}$ at which the FET is just on the verge of switching on is the threshold voltage, $V_{Th}$. Figure 2b shows the transfer characteristics of an n-channel FET indicating the on-state and the off-state. Useful measures with which to assess the switching behaviour are the subthreshold swing, $S$ (relevant to the subthreshold region), and the terminal transconductance, $g_{mt}$ (relevant to the above-threshold region).

In the steady state, a certain number of the MOSFETs in a CMOS logic gate are always switched off so that no current—except the small $I_{off}$—flows through the gate[14]. The ability of silicon MOSFETs to switch off enables silicon CMOS to offer extremely low static power dissipation (which is the reason why silicon CMOS has bested all competing logic technologies). Thus, any successor to the silicon MOSFET that is to be used in CMOS-like logic must have excellent switching capabilities, as well as an on–off ratio, $I_{on}/I_{off}$, of between $10^4$ and $10^7$ (ref. 2). In a conventional FET, this requires semiconducting channels with a sizeable bandgap, preferably 0.4 eV or more. Moreover, n- and p-channel FETs with symmetrical threshold voltages, that is, with $V_{Th,n} = -V_{Th,p}$, are needed for proper CMOS operation.

In radiofrequency applications, however, switch-off is not required *per se*. In small-signal amplifiers, for example, the transistor is operated in the on-state and small radiofrequency signals that are to be amplified are superimposed onto the d.c. gate–source voltage. To discuss the radiofrequency performance of FETs, I use the equivalent circuit from Fig. 3a and focus on the cut-off frequency, $f_T$, which is the frequency at which the magnitude of the small-signal current gain rolls off to unity. The cut-off frequency is the most widely used figure of merit for radiofrequency devices and is, in effect, the highest frequency at which a FET is useful in radiofrequency applications.

As can be seen from the expression for $f_T$ given in Table 1 (refs 7,8), the cut-off frequency can be maximized by making the intrinsic transconductance, $g_m$, as large as possible and making the



© 2010 Macmillan Publishers Limited. All rights reserved

drain conductance, $g_{ds}$, and all the capacitances and resistances in the equivalent circuit (Fig. 3) as small as possible[7,8]. However, the values of all these quantities vary with the applied d.c. gate–source voltage, $V_{GS}$, and the applied d.c. drain–source voltage, $V_{DS}$. As shown exemplarily for a typical GaAs HEMT[15,16] (Fig. 3b,c), $V_{DS}$ has a pronounced effect on the FET performance. For this transistor, $f_T$ peaks around $V_{DS}$ = 1 V, that is, deep in the region of drain-current saturation, where $g_m$ is near its peak and $g_{ds}$ has decreased sufficiently. For lower values of $V_{DS}$, the device operates in the linear regime and the cut-off frequency is low because $g_m$ is small and $g_{ds}$ is large.

The bottom line for radiofrequency performance is that although shorter gates, faster carriers and lower series resistances all lead to higher cut-off frequencies, saturation of the drain current is essential to reach the maximum possible operating speeds. This point is frequently missed in discussions of transistor speeds. Drain-current saturation is also necessary to maximize the intrinsic gain, $G_{int} = g_m/g_{ds}$, which has become a popular figure of merit for mixed-signal circuits.

## Graphene properties relevant to transistors

Single-layer graphene is a purely two-dimensional material. Its lattice consists of regular hexagons with a carbon atom at each corner. The bond length between adjacent carbon atoms, $L_b$, is 1.42 Å and the lattice constant, $a$, is 2.46 Å (Fig. 4a). The first reports on this material appeared decades ago, even before the name graphene had been coined (see, for example, refs 17–19), but it took the pioneering 2004 paper by the Manchester group[1] to spark the present explosion of interest in the material.

At present, the most popular approaches to graphene preparation are mechanical exfoliation[1], growth on metals and subsequent graphene transfer to insulating substrates[20,21], and thermal decomposition of SiC to produce so-called epitaxial graphene on top of SiC wafers[22,23]. Exfoliation is still popular for laboratory use but it is not suited to the electronics industry, whereas the other two options both have the potential for producing wafer-scale graphene. After the graphene has been prepared, common semiconductor processing techniques (such as lithography, metallization and etching) can be applied to fabricate graphene transistors.

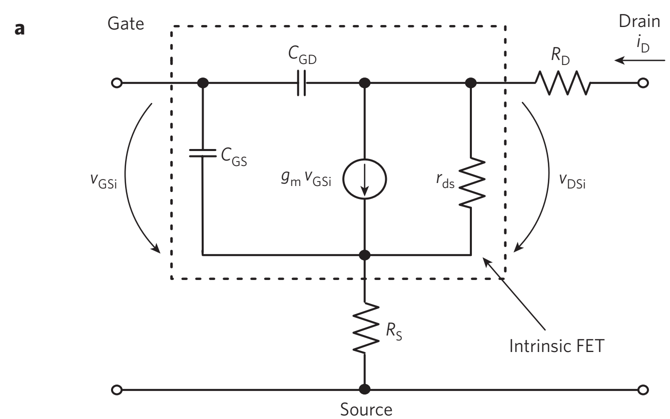
In this section, I discuss two important aspects of graphene: the presence (or otherwise) of a bandgap, and charge transport (mobility and high-field transport) at room temperature.

**Bandgap.** Large-area graphene is a semimetal with zero bandgap. Its valence and conduction bands are cone-shaped and meet at the K points of the Brillouin zone (Fig. 4b). Because the bandgap is zero, devices with channels made of large-area graphene cannot be switched off and therefore are not suitable for logic applications. However, the band structure of graphene can be modified, and it is possible to open a bandgap in three ways: by constraining large-area graphene in one dimension to form graphene nanoribbons, by biasing bilayer graphene and by applying strain to graphene. See Table 2 and refs 24–43 for more details.

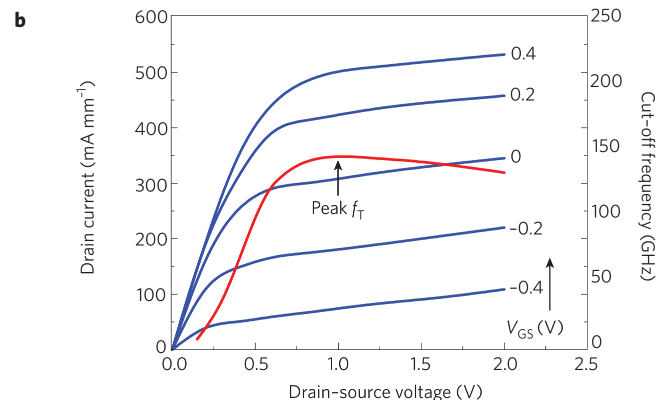
It has been predicted[28] that both armchair nanoribbons and zigzag nanoribbons (the two ideal types of nanoribbon; Fig. 4a) have a bandgap that is, to a good approximation, inversely proportional to the width of the nanoribbon. The opening of a bandgap in nanoribbons has been verified experimentally for widths down to about 1 nm (refs 24–27), and theory and experiments both reveal bandgaps in excess of 200 meV for widths below 20 nm (Fig. 4c). However, it should be noted that real nanoribbons have rough edges and widths that change along their lengths. Even modest edge disorder obliterates any difference in the bandgap between nanoribbons with different edge geometries[29], and edge functionalization and doping can also affect the bandgap[44].

To open a bandgap useful for conventional field-effect devices, very narrow nanoribbons with well-defined edges are needed. This represents a serious challenge given the semiconductor processing

**a**




**b**




**c**

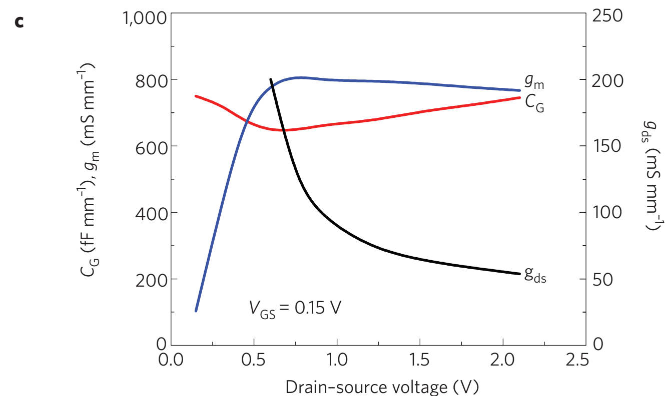



**Figure 3 | FET d.c. and small-signal operation. a**, Small-signal equivalent FET circuit. The intrinsic transconductance, $g_m$, is related to the internal small-signal gate–source and drain–source voltages, $v_{GSi}$ and $v_{DSi}$, whereas the terminal transconductance, $g_{mt}$, is related to the applied gate–source and drain–source voltages, $V_{GS}$ and $V_{DS}$ (Table 1 and Fig. 2b). **b**, The drain current, $I_D$ (blue lines), at different values of $V_{GS}$, and the cut-off frequency, $f_T$ (red line), both versus $V_{DS}$ for a radiofrequency GaAs high-electron-mobility transistor[15,16]. The cut-off frequency peaks at $V_{DS}$ = 1 V and $V_{GS}$ = 0.15 V. **c**, The intrinsic transconductance (blue line), the overall gate capacitance, $C_G = C_{GS} + C_{GD}$ (red line), and the drain conductance, $g_{ds}$ ($1/r_{ds}$; black line), versus $V_{DS}$ for the same FET.

equipment available at the moment. Recently, nanoribbons that were uniform in width and had reduced edge roughness were produced by 'unzipping' carbon nanotubes[45]. However, even a perfect nanoribbon is not perfect for electronics applications. In general, the larger the bandgap that opens in a nanoribbon, the more the



© 2010 Macmillan Publishers Limited. All rights reserved

**Table 1 | Performance measures for the field-effect transistor.**

| Quantity | Definition |
|---|---|
| Terminal transconductance | $g_{mt} = \left.\frac{dI_D}{dV_{GS}}\right\|_{V_{DS} = \text{const}}$ |
| Intrinsic transconductance | $g_m = \left.\frac{dI_D}{dV_{GSi}}\right\|_{V_{DSi} = \text{const}}$ |
| Drain conductance | $g_{ds} = \frac{1}{r_{ds}} = \left.\frac{dI_D}{dV_{DSi}}\right\|_{V_{GSi} = \text{const}}$ |
| Gate–source capacitance | $C_{GS} = -\left.\frac{dQ_{ch}}{dV_{GSi}}\right\|_{V_{DSi} = \text{const}}$ |
| Gate–drain capacitance | $C_{GD} = -\left.\frac{dQ_{ch}}{dV_{DSi}}\right\|_{V_{GSi} = \text{const}}$ |
| Cut-off frequency | $f_T \approx \frac{g_m}{2\pi} \frac{1}{(C_{GS} + C_{GD})[1 + g_{ds}(R_S + R_D)] + C_{GD}g_m(R_S + R_D)}$ |
| Field-effect mobility | $\mu_{FE} = \frac{L_{ch}g_m}{W_{ch}C_G V_{DS}}$ |

$V_{GS}$, $V_{DS}$: terminal d.c. voltages; $V_{GSi}$, $V_{DSi}$: intrinsic d.c. voltages; $Q_{ch}$: mobile channel charge; $L_{ch}$, $W_{ch}$: channel length and width; $C_G$: gate capacitance. In the expression for $\mu_{FE}$, $C_G$ is the gate capacitance per unit area. $R_S$ and $R_D$ are the source and drain series resistances, respectively. Expressions for the terminal and intrinsic transconductances, drain conductance, gate–source and gate–drain capacitances, and cut-off frequency for the equivalent FET circuit shown in Fig. 3a[7,8]. The expression for the field-effect mobility in MOS channels is also shown[66].

valence and conduction bands become parabolic (rather than cone-shaped): this decreases the curvature around the K point and increases the effective mass of the charge carriers[46], which is likely to decrease the mobility.

Bilayer graphene is also gapless (Fig. 4b), and its valence and conduction bands have a parabolic shape near the K point. If an electric field is applied perpendicular to the bilayer, a bandgap opens and the bands near the K point take on the so-called Mexican-hat shape. This opening was predicted by theory[30,31] and has been verified in experiments[32,33]. Theoretical investigations have also shown that the size of the bandgap depends on the strength of the perpendicular field and can reach values of 200–250 meV for high fields ($(1\text{–}3) \times 10^7$ V cm$^{-1}$; refs 30,31).

The bandgap of large-area single-layer epitaxial graphene is at present the subject of controversy[34]. Although some results suggest a zero bandgap[37,38], others report a bandgap of around 0.25 eV (refs 35,36). The transfer characteristics of epitaxial-graphene MOSFETs show no switch-off, which suggests a zero bandgap. However, a bandgap is consistently observed for epitaxial bilayer graphene[38,39].

Finally, strain has been discussed as a means of opening a bandgap in large-area graphene, and the effect of uniaxial strain on the band structure has been simulated[40,41]. At present it seems that if it is possible at all, opening a gap in this way will require a global uniaxial strain exceeding 20%, which will be difficult to achieve in practice. Moreover, little is known about the ways in which other types of strain, such as biaxial strain and local strain, influence the band structure of graphene.

Thus, although there are a number of techniques for opening a bandgap in graphene, they are all at the moment some way from being suitable for use in real-world applications.

**Mobility.** The most frequently stated advantage of graphene is its high carrier mobility at room temperature. Mobilities of 10,000–15,000 cm$^2$ V$^{-1}$ s$^{-1}$ are routinely measured for exfoliated graphene on $SiO_2$-covered silicon wafers[1,47], and upper limits of between 40,000 and 70,000 cm$^2$ V$^{-1}$ s$^{-1}$ have been suggested[47,48]. Moreover, in the absence of charged impurities and ripples, mobilities of 200,000 cm$^2$ V$^{-1}$ s$^{-1}$ have been predicted[49], and a mobility of $10^6$ cm$^2$ V$^{-1}$ s$^{-1}$ was recently reported for suspended graphene[50]. For large-area graphene grown on nickel and transferred to a substrate, mobilities greater than 3,700 cm$^2$ V$^{-1}$ s$^{-1}$ have been measured[20].

Finally, for epitaxial graphene on silicon carbide, the mobility depends on whether the graphene is grown on the silicon face or the carbon face of SiC. Although graphene grown on the carbon face has higher mobility (values of ~5,000 cm$^2$ V$^{-1}$ s$^{-1}$ have been reported[23], compared with ~1,000 cm$^2$ V$^{-1}$ s$^{-1}$ for graphene grown on the silicon face[23,51]), it is easier to grow single-layer and bilayer graphene on the silicon face, which makes the silicon face of SiC more suited for electronic applications.

In early graphene MOS structures, the mobility was affected by the use of a top-gate dielectric[52,53]. However, the recent demonstration of mobilities of around 23,000 cm$^2$ V$^{-1}$ s$^{-1}$ in top-gated graphene MOS channels[54] and the observation of similar mobilities before and after top-gate formation[55] show that high-mobility graphene



© 2010 Macmillan Publishers Limited. All rights reserved

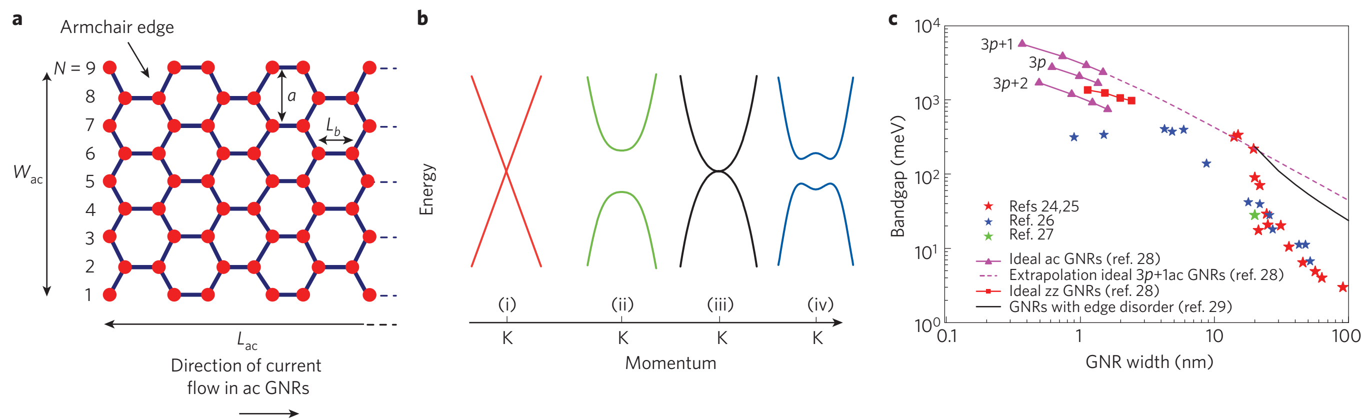



**Figure 4 | Properties of graphene and graphene nanoribbons. a**, Schematic of an armchair (ac) graphene nanoribbon (GNR) of length $L_{ac}$ and width $W_{ac}$. The nanoribbon shown here has $N = 9$ carbon atoms along its width and thus belongs to the 3*p* family, where *p* is an integer. **b**, Band structure around the K point of (i) large-area graphene, (ii) graphene nanoribbons, (iii) unbiased bilayer graphene, and (iv) bilayer graphene with an applied perpendicular field. Large-area graphene and unbiased bilayer graphene do not have a bandgap, which makes them less useful for digital electronics. **c**, Bandgap versus nanoribbon width from experiments[24–27] and calculations[28,29]. By comparison, the bandgap of Si is above 1 eV. zz: zigzag.

MOS channels can be made with a proper choice of the gate dielectric and optimization of the deposition process.

These mobility numbers are impressive, but they require closer inspection. The high mobilities mentioned above relate to large-area graphene, which is gapless. A general trend for conventional semiconductors is that the electron mobility decreases as the bandgap increases, and a similar trend has been predicted for carbon nanotubes (CNTs)[56,57] and graphene nanoribbons[58–61] (Fig. 5a). This means that the mobility in nanoribbons with a bandgap similar to that of silicon (1.1 eV) is expected to be lower than in bulk silicon and no higher than the mobility in the silicon channel of a conventional MOS device[58]. The mobilities measured in experiments—less than 200 $cm^2 V^{-1} s^{-1}$ for nanoribbons 1–10 nm wide[26,62] and 1,500 $cm^2 V^{-1} s^{-1}$ for a nanoribbon 14 nm wide[45] (which is the highest mobility so far measured for a nanoribbon)—support the theoretical results (Fig. 5b). Therefore, although the high mobilities offered by graphene can increase the speed of devices, they come at the expense of making it difficult to switch devices off, thus removing one of the main advantages of the CMOS configuration—its low static power consumption.

**High-field transport.** In the days when FETs had gates several micrometres long, the mobility was the appropriate measure of the speed of carrier transport. Strictly speaking, however, the mobility describes carrier transport in low electric fields; the short gate lengths in modern FETs result in high fields in a sizeable portion of the channel, reducing the relevance of mobility to device performance. To illustrate this, let us consider a FET with a gate 100 nm long and a drain–source voltage of 1 V. If we assume a voltage drop of 0.3 V across the series resistances, the average field in the channel is 70 kV $cm^{-1}$. At such high fields, the steady-state carrier velocity saturates, and this saturation velocity becomes another important measure of carrier transport. Figure 5c shows plots of the electron velocity versus the electric field for conventional semiconductors, and simulated plots for large-area graphene[63,64] and a carbon nanotube[57]. For graphene and the nanotube, maximum carrier velocities of around $4 \times 10^7$ cm $s^{-1}$ are predicted, in comparison with $2 \times 10^7$ cm $s^{-1}$ for GaAs and $10^7$ cm $s^{-1}$ for silicon. Moreover, at high fields the velocity in graphene and the nanotube does not drop as drastically as in the III–V semiconductors. Unfortunately, there is at present no experimental data available on high-field transport in graphene nanoribbons and in large-area graphene. However, other measurements[65] suggest high-field carrier velocities of several $10^7$ cm $s^{-1}$ in graphene. Thus, regarding high-field transport, graphene and nanotubes seem to have a slight advantage over conventional semiconductors.

Finally, it is worth noting that reported mobilities for graphene devices need to be interpreted carefully because there are several

**Table 2 | Does graphene have a bandgap?**

| Graphene type | Size | Bandgap | Remarks | Ref. |
|---|---|---|---|---|
| SL graphene on $SiO_2$ | LA | No | Experiment and theory | 1, 5 |
| SL graphene on $SiO_2$ | GNR | Yes | Experiment and theory; gap due to lateral confinement* | 24–29 |
| BL graphene on $SiO_2$ | LA | Yes | Experiment and theory; gap due to symmetry breaking by perpendicular interlayer field | 30–33 |
| Epitaxial SL | LA | Unknown | Controversial discussion | 34 |
| | | Yes | Experiment and theory, gap due to symmetry breaking | 35, 36 |
| | | No | Experiment and theory | 37, 38 |
| Epitaxial BL | LA | Yes | Experiment and theory | 32, 38, 39 |
| Epitaxial SL, BL | GNR | Yes | Theory | 39 |
| Strained SL† | LA | Yes | Theory; gap due to level crossing | 40 |
| | | No | Theory | 41 |

SL: single-layer; BL: bilayer; LA: large-area; GNR: graphene nanoribbon. *The origin of the bandgap in nanoribbons is still under debate: in addition to pure lateral confinement[28], it has been suggested that the Coulomb blockade[42,43] or Anderson localization[29] might be responsible for the formation of the gap. †Theorists disagree about the existence of a bandgap for strained SL graphene.



© 2010 Macmillan Publishers Limited. All rights reserved

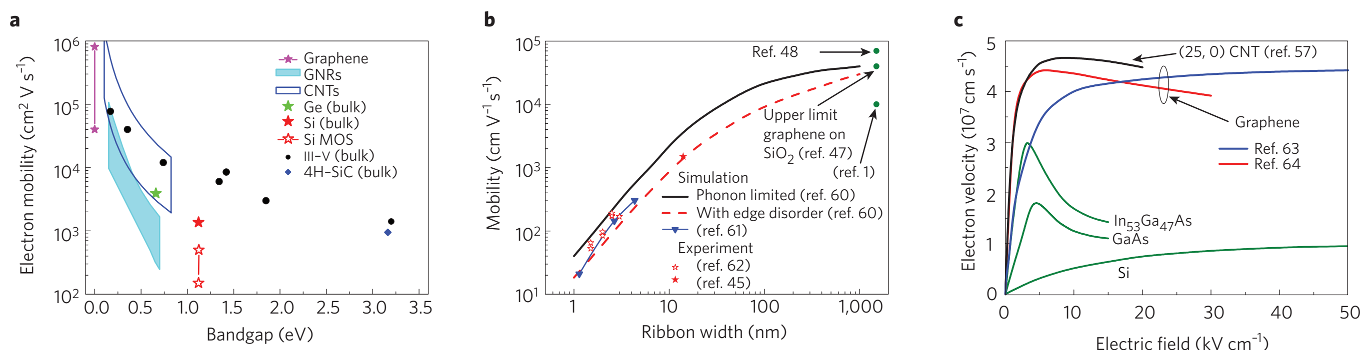



**Figure 5 | Carrier transport in graphene. a**, Electron mobility versus bandgap in low electric fields for different materials, as indicated (from left to right, III-V compounds are InSb, InAs, $In_{0.53}Ga_{0.47}As$, InP, GaAs, $In_{0.49}Ga_{0.51}P$, and GaN). The mobility data relates to undoped material except for the Si MOS data. Also shown are mobility data for carbon nanotubes (CNTs; simulation[56,57]), graphene nanoribbons (simulation[58,59]) and graphene (experiment and simulation[47–50]). **b**, Carrier mobility versus nanoribbon width at low electric fields from simulations[60,61] and experiments (open[62] and full[45] stars). Data for large-area graphene are also shown[1,47,48]. **c**, Electron drift velocity versus electric field for common semiconductors (Si, GaAs, $In_{0.53}Ga_{0.47}As$), a carbon nanotube (simulation[57]) and large-area graphene (simulation[63,64]).

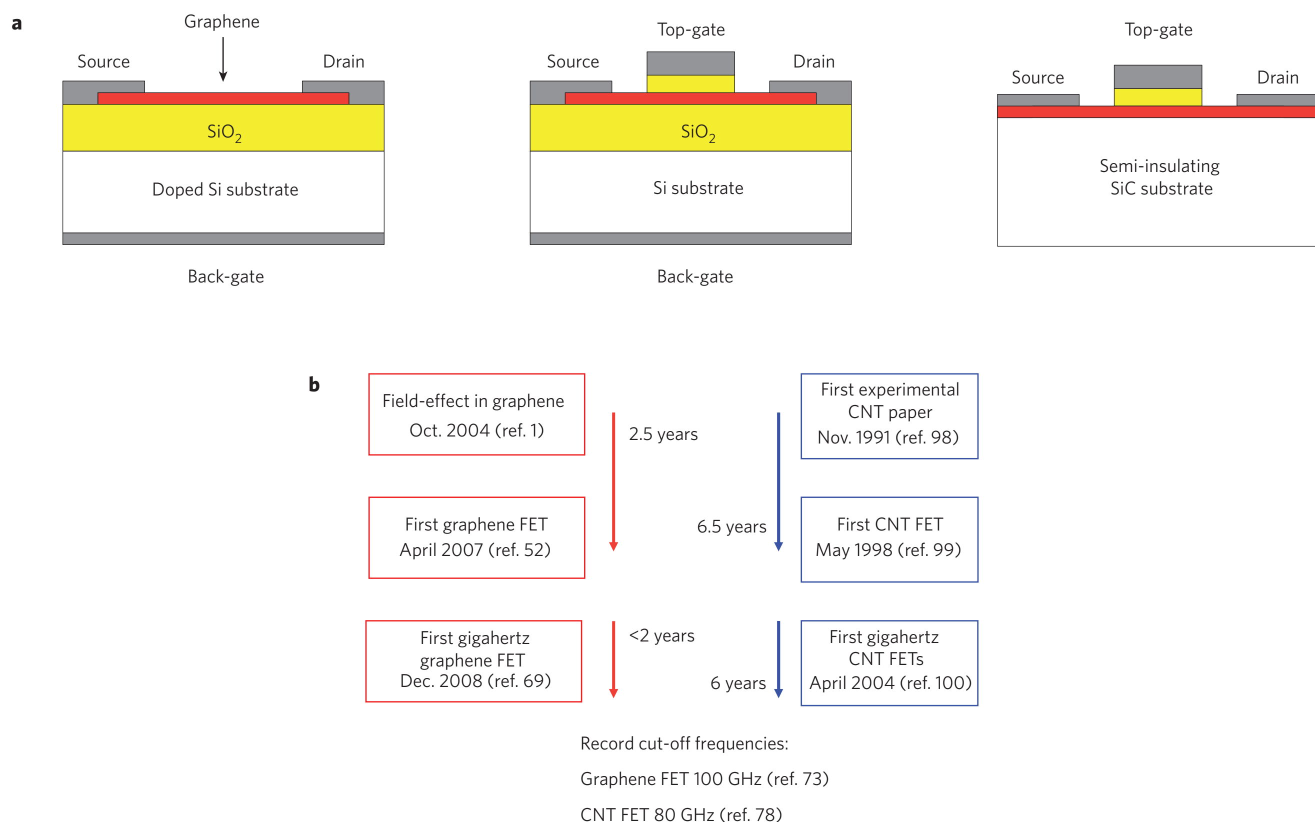



**Figure 6 | Structure and evolution of graphene MOSFETs. a**, Schematics of different graphene MOSFET types: back-gated MOSFET (left); top-gated MOSFET with a channel of exfoliated graphene or of graphene grown on metal and transferred to a $SiO_2$-covered Si wafer (middle); top-gated MOSFET with an epitaxial-graphene channel (right). The channel shown in red can consist of either large-area graphene or graphene nanoribbons. **b**, Progress in graphene MOSFET development[1,52,69,73] compared with the evolution of nanotube FETs[78,98–100].

definitions for the MOSFET channel mobility and they are difficult to compare[66]. Furthermore, the techniques used to measure mobility are only vaguely described in some papers. Most frequently, the field-effect mobility, $\mu_{FE}$, is measured (Table 1). However, the effect of the source and drain series resistances must be eliminated from the measured characteristics to determine this quantity, and it is not always clear that this has been done.

An additional complication lies in the interpretation of data from top-gated graphene MOSFETs, which involves arriving at a value for the gate capacitance, $C_G$. Frequently $C_G$ is approximated by the oxide capacitance per unit area, as $C_{ox} = \varepsilon_{ox}/t_{ox}$, where $\varepsilon_{ox}$ is the dielectric constant of the top-gate dielectric and $t_{ox}$ is the thickness of this dielectric. However, when $t_{ox}$ is small, the quantum capacitance, $C_q$, must be taken into account[67,68] because it is connected in series with $C_{ox}$, making the overall gate capacitance $C_G = C_{ox}C_q/(C_{ox} + C_q)$. The overall gate capacitance can be significantly smaller than $C_{ox}$, particularly close to the Dirac point (the point of minimum drain current), so neglecting the effect of $C_q$ will lead to an underestimate of the field-effect mobility.



© 2010 Macmillan Publishers Limited. All rights reserved

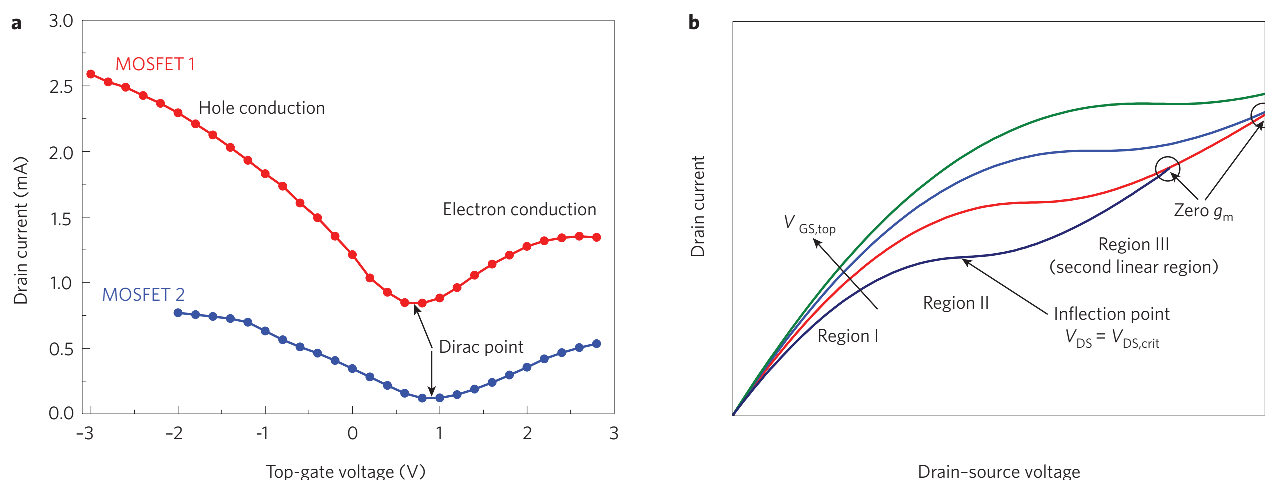



**Figure 7 | Direct-current behaviour of graphene MOSFETs with a large-area-graphene channel. a**, Typical transfer characteristics for two MOSFETs with large-area-graphene channels[23,71]. The on–off ratios are about 3 (MOSFET 1) and 7 (MOSFET 2), far below what is needed for applications in logic circuits. Unlike conventional Si MOSFETs, current flows for both positive and negative top-gate voltages. **b**, Qualitative shape of the output characteristics (drain current, $I_D$, versus drain–source voltage, $V_{DS}$) of a MOSFET with an n-type large-area-graphene channel, for different values of the top-gate voltage, $V_{GS,top}$. Saturation behaviour can be seen. At sufficiently large $V_{DS}$ values, the output characteristics for different $V_{GS,top}$ values may cross[75], leading to a zero or even negative transconductance, which means that the gate has effectively lost control of the current.

## State of the art of graphene transistors

A graphene MOS device was among the breakthrough results reported by the Manchester group in 2004 (ref. 1). A 300-nm $SiO_2$ layer underneath the graphene served as a back-gate dielectric and a doped silicon substrate acted as the back-gate (Fig. 6a). Such back-gate devices have been very useful for proof-of-concept purposes, but they suffer from unacceptably large parasitic capacitances and cannot be integrated with other components. Therefore, practical graphene transistors need a top-gate. The first graphene MOSFET with a top-gate was reported in 2007 (ref. 52), representing an important milestone, and progress has been very rapid since then (Fig. 6b). Although research into graphene is still in its infancy, graphene MOSFETs can compete with devices that have benefited from decades of research and investment.

Top-gated graphene MOSFETs have been made with exfoliated graphene[52–55,69,70], graphene grown on metals such as nickel and copper[71,72], and epitaxial graphene[23,73,74]; $SiO_2$, $Al_2O_3$, and $HfO_2$ have been used for the top-gate dielectric. The channels of these top-gated graphene transistors have been made using large-area graphene, which does not have a bandgap, so they have not been able to switch off.

Large-area-graphene transistors have a unique current–voltage transfer characteristic (Fig. 7a). The carrier density and the type of carrier (electrons or holes) in the channel are governed by the potential differences between the channel and the gates (top-gate and/or back-gate). Large positive gate voltages promote an electron accumulation in the channel (n-type channel), and large negative gate voltages lead to a p-type channel. This behaviour gives rise to the two branches of the transfer characteristics separated by the Dirac point (Fig. 7a). The position of the Dirac point depends on several factors: the difference between the work functions of the gate and the graphene, the type and density of the charges at the interfaces at the top and bottom of the channel (Fig. 6), and any doping of the graphene. The on–off ratios reported for MOSFET devices with large-area-graphene channels are in the range 2–20.

The output characteristics of many graphene MOSFETs either show a linear shape without any saturation[53] or only weak saturation[73,74], each of which is a disadvantage with respect to device speed. However, some graphene MOSFETs have an unusual form of saturation-like behaviour that includes a second linear region[70,71,75] (Fig. 7b). Our present understanding of the origin of this behaviour is as follows. For small values of $V_{DS}$, the transistor operates in the linear region and the entire channel is n-type (region I). As $V_{DS}$ is increased, the drain current starts to saturate until the inflection point at $V_{DS} = V_{DS,crit}$ is reached (region II). At this point, the potential conditions at the drain end of the channel correspond to the Dirac point. Once $V_{DS}$ exceeds $V_{DS,crit}$, the conduction type at the drain end of the channel switches from n-type to p-type[70,76] and the transistor enters a second linear region (region III). At sufficiently large values of $V_{DS}$, the output characteristics for different gate voltages may cross[75], leading to a zero or even negative transconductance—a highly undesirable situation. This peculiar behaviour is a consequence of these devices having gapless channels and does not occur in FETs with semiconducting channels.

Recently, graphene MOSFETs with gigahertz capabilities have been reported. These transistors possess large-area channels of exfoliated[53,55,69,77] and epitaxial[73,74] graphene. The fastest graphene transistor currently is a MOSFET with a 240-nm gate that has a cut-off frequency of $f_T$ = 100 GHz (ref. 73), which is higher than those of the best silicon MOSFETs with similar gate lengths (as is the cut-off frequency of 53 GHz reported for a device with a 550-nm gate, also in ref. 73). A weak point of all radiofrequency graphene MOSFETs reported so far is the unsatisfying saturation behaviour (only weak saturation or the second linear regime), which has an adverse impact on the cut-off frequency, the intrinsic gain and other figures of merit for radiofrequency devices. However, outperforming silicon MOSFETs while operating with only weak current saturation[73] is certainly impressive.

Figure 8 shows the cut-off frequency for a variety of devices including graphene MOSFETs, nanotube FETs, and various radiofrequency FETs. For conventional radiofrequency FETs with gate lengths greater than 0.2 μm, the $f_T$ data for each transistor type has an $L^{-1}$ dependence, where $L$ is the gate length. Furthermore, $f_T$ increases with mobility[9]. Silicon MOSFETs show channel mobilities of a few 100 $cm^2 V^{-1} s^{-1}$ compared with about 6,000 $cm^2 V^{-1} s^{-1}$ for GaAs pHEMTs and more than 10,000 $cm^2 V^{-1} s^{-1}$ for InP HEMTs and GaAs mHEMTs. At shorter gate lengths, however, the mobility becomes less important for transistor speed and the deleterious influence of parasitic resistances and short-channel effects increases. Both nanotube and graphene FETs are still slower than



© 2010 Macmillan Publishers Limited. All rights reserved

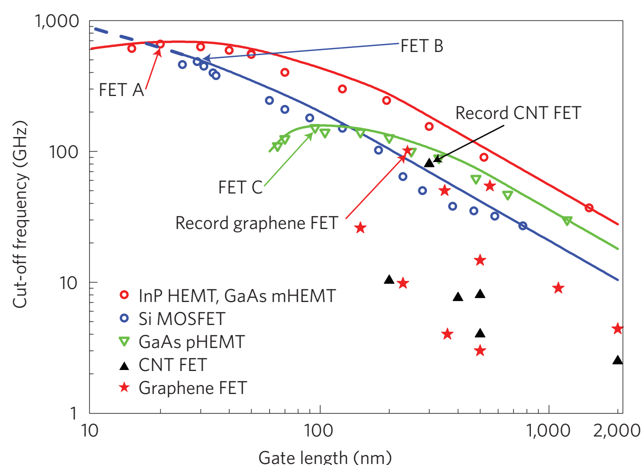



**Figure 8 | Comparing cut-off frequencies for different FETs.** Cut-off frequency versus gate length for graphene MOSFETs, nanotube FETs and three types of radiofrequency FET; the symbols are experimental data points and the lines are a guide to the eye for type A (InP HEMT and GaAs mHEMT), B (Si MOSFET) and C (GaAs pHEMT) devices (as indicated). The FET A with the highest cut-off frequency (660 GHz) is a GaAs metamorphic HEMT (mHEMT) with a 20-nm gate (M. Schlechtweg, personal communication). The FET B with the highest cut-off frequency (485 GHz) is a Si MOSFET with a 29-nm gate[101]. The FET C with the highest cut-off frequency (152 GHz) is a GaAs pseudomorphic HEMT (pHEMT) with a 100-nm gate[102]. The fastest nanotube device (CNT FET) has $f_T$ = 80 GHz and $L$ = 300 nm (ref. 78), and the fastest reported graphene MOSFET has $f_T$ = 100 GHz and $L$ = 240 nm (ref. 73).

the best conventional radiofrequency FETs, but they have recently overtaken the best silicon MOSFETs with gate lengths above 200 nm and are approaching the performance of GaAs pHEMTs. (See ref. 78 for details of the nanotube with the highest $f_T$ reported so far, and ref. 79 for more information on the radiofrequency potential of nanotube FETs.)

Although the low on–off ratios demonstrated so far make use in logic devices unrealistic, transistors with large-area graphene channels are promising candidates for radiofrequency applications because radiofrequency FETs are not required to switch off and can benefit from the high mobilities offered by large-area graphene. However, the absence of drain-current saturation will limit the radiofrequency performance of graphene transistors.

One method of introducing a bandgap into graphene for logic applications is to create graphene nanoribbons. Nanoribbon MOSFETs with back-gate control and widths down to less than 5 nm have been operated as p-channel devices and had on–off ratios of up to $10^6$ (refs 26,62). Such high ratios have been obtained despite simulations showing that edge disorder leads to an undesirable decrease in the on-currents and a simultaneous increase in the off-current of nanoribbon MOSFETs[80,81].This, and other evidence of a sizeable bandgap opening in narrow nanoribbons, provides proof of the suitability of nanoribbon FETs for logic applications. However, these devices had relatively thick back-gate oxides, so voltage swings of several volts were needed for switching, which is significantly more than the swings of 1 V and less needed to switch Si CMOS devices[2]. Furthermore, CMOS logic requires both n-channel and p-channel FETs with well-controlled threshold voltages, and graphene FETs with all these properties have not yet been reported.

Recently, the first graphene nanoribbon MOSFETs with top-gate control have been reported[82]. These transistors feature a thin high-dielectric-constant (high-$k$) top-gate dielectric (1–2 nm of $HfO_2$), a room-temperature on–off ratio of 70 and an outstanding transconductance of 3.2 mS μm$^{-1}$ (which is higher than the transconductances reported for state-of-the-art silicon MOSFETs and III–V HEMTs).

Graphene bilayer MOSFETs have been investigated experimentally[83] and by device simulation[84]. Although the on–off ratios reported so far (100 at room temperature and 2,000 at low temperature[83]) are too small for logic applications, they mark a significant improvement (of about a factor of 10) over MOSFETs in which the channel is made of large-area gapless graphene.

The contact resistance between the metallic source and drain contacts and the graphene channel should be briefly mentioned. So far, the lowest reported metal–graphene contact resistances are in the range 500–1,000 Ω cm (refs 85,86), which is about ten times the contact resistance of silicon MOSFETs and III–V HEMTs[8,13]. Remarkably, in spite of the importance of the contacts (particularly for short-channel devices), only a few studies dealing with metal–graphene contacts have been published[85–87] and more work is needed to understand the contact properties.

I now return to the two-dimensional nature of graphene. According to scaling theory, as noted previously, a thin channel region allows short-channel effects to be suppressed and thus makes it feasible to scale MOSFETs to very short gate lengths. The two-dimensional nature of graphene means it offers us the thinnest possible channel, so graphene MOSFETs should be more scalable than their competitors. It should be noted, however, that scaling theory is valid only for transistors with a semiconducting channel and does not apply to graphene MOSFETs with gapless channels. Thus, the scaling theory does describe nanoribbon MOSFETs, which have a bandgap but which have significantly lower mobilities than large-area graphene, as discussed. Given that the high published values of mobility relate to gapless large-area graphene, the most attractive characteristic of graphene for use in MOSFETs, in particular those required to switch off, may be its ability to scale to shorter channels and higher speeds, rather than its mobility.

## Further options for graphene devices

It has become clear that graphene devices based on the conventional MOSFET principle suffer from some fundamental problems. This has motivated researchers to explore new graphene device concepts, such as tunnel FETs and bilayer pseudospin FETs. In a tunnel FET, the band-to-band tunnelling across the source–channel junction can be controlled using the gate–source voltage. The big advantage of tunnel FETs is that their subthreshold swings are not limited to 60 mV per decade, as in conventional MOSFETs[7,10], which should lead to steeper subthreshold characteristics and better switch-off. The tunnel-FET approach has already been explored in silicon and carbon-nanotube MOSFETs[88,89]. Tunnel FETs based on nanoribbons and bilayer graphene have been investigated in simulations[84,90,91] but have not been demonstrated experimentally. In particular, the bilayer graphene tunnel FET is now considered to be a promising device for a number of reasons: narrow nanoribbons are not needed, so edge disorder will not be a problem and patterning will be relatively easy; the small bandgap opened by a vertical field applied across the two layers is sufficient to suppress band-to-band tunnelling in the off-state and thus enables effective switch-off; and the possibility of subthreshold swings below 60 mV per decade should make high on–off ratios possible[84].

The bilayer pseudospin FET consists of a vertical stack of two graphene layers separated by a thin dielectric[92]. Under certain bias conditions the tunnelling resistance between the two graphene layers becomes so small that the layers are effectively shorted, causing the FET to pass a high current, whereas under other conditions the tunnelling resistance is very large, shutting the current off. The bilayer pseudospin FET might therefore be able to deliver fast and ultralow-power logic operation.



© 2010 Macmillan Publishers Limited. All rights reserved

Although graphene tunnel FETs and bilayer pseudospin FETs are both still at an embryonic stage, they have already gained considerable attention in the electron-device community and have been included in the chapter on emerging research devices in the latest edition of the ITRS[2]. It might also be possible to make interconnects from graphene, which would open the possibility of all-graphene integrated circuits in which both the active devices and the wiring were made of graphene[22]. It has been shown that graphene interconnects compete well with copper interconnects[93,94]; indeed, graphene can support current densities greater than $10^8$ A $cm^{-2}$ (which is 100 times higher than those supported by copper and is comparable with those supported by nanotubes)[95] and has a thermal conductivity of around 30–50 W $cm^{-1}$ $K^{-1}$ (in comparison with 4 W $cm^{-1}$ $K^{-1}$ for copper)[96].

## Outlook

Since 2007, we have witnessed huge progress in the development of graphene transistors. Most impressive were the demonstrations of a graphene MOSFET with a cut-off frequency of 100 GHz (ref. 73), the excellent switching behaviour of nanoribbon MOSFETs[26,62], and channel mobilities exceeding 20,000 $cm^2$ $V^{-1}$ $s^{-1}$ in top-gated graphene MOSFETs[54]. However, this progress has been accompanied by the appearance of a number of problems. MOSFETs with large-area-graphene channels cannot be switched off, making them unsuitable for logic applications, and their peculiar saturation behaviour limits their radiofrequency performance. Nanoribbon graphene, which does have a bandgap and results in transistors that can be switched off, has serious fabrication issues because of the small widths required and the presence of edge disorder.

The primary challenges facing the community at present, therefore, are to create in a controlled and practical fashion a bandgap in graphene, which would allow logic transistors to switch off and radiofrequency transistors to avoid the second linear regime (Fig. 7b), and to develop other means of improving transistor saturation characteristics by, for example, developing contacts that block one kind of carrier without degrading the transistor's speed. The community may also benefit from recognizing that the motivation to use graphene in transistors in the first place stems less from ultrahigh mobilities than from graphene's ability to scale to short gate lengths and high speeds by virtue of its thinness.

This discussion of the problems of graphene MOSFETs should not lead to the conclusion that graphene is not a promising material for transistors. Rather, I have chosen a more critical view to avoid a situation that has been seen in the past, in which a new device or material concept has been prematurely declared capable of replacing the status quo. Also, I agree with David Ferry, a veteran of semiconductor device research, when he says that[97] "many such saviours have come and gone, yet the reliable silicon CMOS continues to be scaled and to reach even higher performance levels".

I conclude by noting that the first top-gated graphene transistors were reported only three years ago. Given this short history, and given that all other possible successors to conventional mainstream transistors also face serious problems, we cannot help but be impressed with the rapid development of graphene. Concepts that have been investigated for many years, such as spin transistors or molecular devices, seem to be farther from real application than does graphene, and it is not clear if they will ever reach the production stage. At the moment, it is impossible to say which, if any, of the alternative device concepts being considered will replace conventional transistors. However, the latest ITRS roadmap strongly recommends intensified research into graphene and even contains a research and development schedule for carbon-based nanoelectronics[2]. The race is still open and the prospects for graphene devices are at least as promising as those for alternative concepts.

## References


1. Novoselov, K. S. *et al.* Electric field effect in atomically thin carbon films. *Science* **306,** 666–669 (2004).
2. *The International Technology Roadmap for Semiconductors* http://www.itrs.net/Links/2009ITRS/Home2009.htm (Semiconductor Industry Association, 2009).
3. Geim, A. K. & Novoselov, K. S. The rise of graphene. *Nature Mater.* **6,** 183–191 (2007).
4. Geim, A. K. Graphene: status & prospects. *Science* **324,** 1530–1534 (2009).
5. Castro Neto, A. H. *et al.* The electronic properties of graphene. *Rev. Mod. Phys.* **81,** 109–162 (2009).
6. Moore, G. E. in *Tech. Dig. ISSCC* 20–23 (IEEE, 2003).
7. Schwierz, F., Wong, H. & Liou, J. J. *Nanometer CMOS* (Pan Stanford, 2010).
8. Schwierz, F. & Liou, J. J. *Modern Microwave Transistors – Theory, Design, and Performance* (Wiley, 2003).
9. Schwierz, F. & Liou, J. J. RF transistors: recent developments and roadmap toward terahertz applications. *Solid-State Electron.* **51,** 1079–1091 (2007).
10. Taur, Y. & Ning, T. H *Fundamentals of Modern VLSI Devices* (Cambridge Univ. Press, 1998).
11. Frank, D. J., Taur, Y. & Wong, H-S. P. Generalized scale length for two-dimensional effects in MOSFETs. *IEEE Electron Dev. Lett.* **19,** 385–387 (1998).
12. Aberg, I. & Hoyt, J. L. Hole transport in ultra-thin-body MOSFETs in strained-Si directly on insulator with strained-Si thickness less than 5 nm. *IEEE Electron Dev. Lett.* **26,** 661–663 (2005).
13. Thompson, S. E. *et al.* In search of "forever", continued transistor scaling one new material at a time. *IEEE Trans. Semicond. Manuf.* **18,** 26–36 (2005).
14. Uyemura, J. P. *CMOS Logic Circuit Design* (Kluwer Academic, 1999).
15. Hughes, B. & Tasker, P. J. Bias dependence of the MODFET intrinsic model elements values at microwave frequencies. *IEEE Trans. Electron. Dev.* **36,** 2267–2273 (1989).
16. Nguyen, L. D. *et al.* in *Tech. Dig. IEDM* 176–179 (IEEE, 1988).
17. Boehm, H. P., Clauss, A., Hofmann, U. & Fischer, G. O. Dünnste Kohlenstoff-Folien. *Z. Naturforsch. B* **17,** 150–153 (1962).
18. May, J. W. Platinum surface LEED rings. *Surf. Sci.* **17,** 267–270 (1969).
19. van Bommel, A. J., Crombeen, J. E. & van Tooren, A. LEED and Auger electron observations of the SiC (0001) surface. *Surf. Sci.* **48,** 463–472 (1975).
20. Kim, K-S. *et al.* Large-scale pattern growth of graphene films for stretchable transparent electrodes. *Nature* **457,** 706–710 (2009).
21. Reina, A. *et al.* Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition. *Nano Lett.* **9,** 30–35 (2009).
22. Berger, C. *et al.* Electronic confinement and coherence in patterned epitaxial graphene. *Science* **312,** 1191–1196 (2006).
23. Kedzierski, J. *et al.* Epitaxial graphene transistors on SiC substrates. *IEEE Trans. Electron. Dev.* **55,** 2078–2085 (2008).
24. Han, M. *et al.* Energy band-gap engineering of graphene nanoribbons. *Phys. Rev. Lett.* **98,** 206805 (2007).
25. Kim, P. *et al.* in *Tech. Dig. IEDM* 241–244 (IEEE, 2009).
26. Li, X., Wang, X., Zhang, L., Lee, S. & Dai, H. Chemically derived, ultrasmooth graphene nanoribbon semiconductors. *Science* **319,** 1229–1232 (2008).
27. Chen, Z., Lin, Y-M., Rooks, M. J. & Avouris, Ph. Graphene nano-ribbon electronics. *Physica E* **40,** 228–232 (2007).
28. Yang, L. *et al.* Quasiparticle energies and band gaps in graphene nanoribbons. *Phys. Rev. Lett.* **99,** 186801 (2007).
29. Evaldsson, M., Zozoulenko, I. V., Xu, H. & Heinzel, T. Edge-disorder-induced Anderson localization and conduction gap in graphene nanoribbons. *Phys. Rev. B* **78,** 161407 (2008).
30. Castro, E. V. *et al.* Biased bilayer graphene: semiconductor with a gap tunable by the electric field effect. *Phys. Rev. Lett.* **99,** 216802 (2007).
31. Gava, P., Lazzeri, M., Saitta, A. M. & Mauri, F. *Ab initio* study of gap opening and screening effects in gated bilayer graphene. *Phys. Rev. B* **79,** 165431 (2009).
32. Ohta, T., Bostwick, A., Seyller, Th., Horn, K. & Rotenberg, E. Controlling the electronic structure of bilayer graphene. *Science* **313,** 951–954 (2006).
33. Zhang, Y. *et al.* Direct observation of a widely tunable bandgap in bilayer graphene. *Nature* **459,** 820–823 (2009).
34. Rotenberg, E. *et al.* and Zhou, S. Y. *et al.* Origin of the energy bandgap in epitaxial graphene. *Nature Mater.* **7,** 258–260 (2008).
35. Zhou, S. Y. *et al.* Substrate-induced bandgap opening in epitaxial graphene. *Nature Mater.* **6,** 770–775 (2007).
36. Kim, S., Ihm, J., Choi, H. J. & Son, Y-W. Origin of anomalous electronic structures of epitaxial graphene on silicon carbide. *Phys. Rev. Lett.* **100,** 176802 (2008).
37. Bostwick, A., Ohta, T., Seyller, Th., Horn, K. & Rotenberg, E. Quasiparticle dynamics in graphene. *Nature Phys.* **3,** 36–40 (2007).
38. Peng, X. & Ahuja, R. Symmetry breaking induced bandgap in epitaxial graphene layers on Si. *Nano Lett.* **8,** 4464–4468 (2008).
39. Sano, E. & Otsuji, T. Theoretical evaluation of channel structure in graphene field-effect transistors. *Jpn. J. Appl. Phys.* **48,** 041202 (2009).
40. Pereira, V. M., Castro Neto, A. H. & Peres, N. M. R. Tight-binding approach to uniaxial strain in graphene. *Phys. Rev. B* **80,** 045401 (2009).




© 2010 Macmillan Publishers Limited. All rights reserved

41. Ni, Z. H. *et al.* Uniaxial strain on graphene: Raman spectroscopy study and band-gap opening. *ACS Nano* **2,** 2301–2305 (2008); erratum **3,** 483 (2009).
42. Sols, F., Guinea, F. & Castro Neto, A. H. Coulomb blockade in graphene nanoribbons. *Phys. Rev. Lett.* **99,** 166803 (2007).
43. Han, M. Y., Brant, J. C. & Kim, P. Electron transport in disordered graphene nanoribbons. *Phys. Rev. Lett.* **104,** 056801 (2010).
44. Cervantes-Sodi, F., Csanyi, G., Picanec, S. & Ferrari, A. C. Edge-functionalized and substitutionally doped graphene nanoribbons: electronic and spin properties. *Phys. Rev. B* **77,** 165427 (2008).
45. Jiao, J., Wang, X., Diankov, G., Wang, H. & Dai, H. Facile synthesis of high-quality graphene nanoribbons. *Nature Nanotech.* **5,** 321–325 (2010).
46. Raza, H. & Kan, E. C. Armchair graphene nanoribbons: electronic structure and electric-field modulation. *Phys. Rev. B* **77,** 245434 (2008).
47. Chen, J-H., Jang, C., Xiao, S., Ishigami, M. & Fuhrer, M. S. Intrinsic and extrinsic performance limits of graphene devices on $SiO_2$. *Nature Nanotech.* **3,** 206–209 (2008).
48. Chen, F., Xia, J., Ferry, D. K. & Tao, N. Dielectric screening enhanced performance in graphene FET. *Nano Lett.* **9,** 2571–2574 (2009).
49. Morozov, V. S. *et al.* Giant intrinsic carrier mobilities in graphene and its bilayer. *Phys. Rev. Lett.* **100,** 016602 (2008).
50. Geim, A. Graphene update. *Bull. Am. Phys. Soc.* **55,** abstr. J21.0004, http://meetings.aps.org/link/BAPS.2010.MAR.J21.4 (2010).
51. Emtsev, K. V. *et al.* Towards wafer-size graphene layers by atmospheric pressure graphitization of silicon carbide. *Nature Mater.* **8,** 203–207 (2009).
52. Lemme, M. C., Echtermeyer, T. J., Baus, M. & Kurz, H. A graphene field-effect device. *IEEE Electron Dev. Lett.* **28,** 282–284 (2007).
53. Lin, Y-M. *et al.* Operation of graphene transistors at gigahertz frequencies. *Nano Lett.* **9,** 422–426 (2009).
54. Liao, L. *et al.* High-κ oxide nanoribbons as gate dielectrics for high mobility top-gated graphene transistors. *Proc. Natl Acad. Sci. USA* **107,** 6711–6715 (2010).
55. Farmer, D. B. *et al.* Utilization of a buffered dielectric to achieve high field-effect carrier mobility in graphene transistors. *Nano Lett.* **9,** 4474–4478 (2009).
56. Zhou, X., Park, J-Y., Huang, S., Liu, J. & McEuen, P. L. Band structure, phonon scattering, and performance limit of single-walled carbon nanotube transistors. *Phys. Rev. Lett.* **95,** 146805 (2005).
57. Perebeinos, V., Tersoff, J. & Avouris, Ph. Electron-phonon interaction and transport in semiconducting carbon nanotubes. *Phys. Rev. Lett.* **94,** 0786802 (2005).
58. Obradovic, B. *et al.* Analysis of graphene nanoribbons as a channel material for field-effect transistors. *Appl. Phys. Lett.* **88,** 142102 (2006).
59. Fang, T., Konar, A., Xing, H. & Jena, D. Mobility in semiconducting nanoribbons: phonon, impurity, and edge roughness scattering. *Phys. Rev. B* **78,** 205403 (2008).
60. Bresciani, M., Palestri, P., Esseni, D. & Selmi, L. in *Proc. ESSDERC '09* 480–483 (IEEE, 2009).
61. Betti, A., Fiori, G., Iannaccone, G. & Mao, Y. in *Tech. Dig. IEDM 2009* 897–900 (IEEE, 2009).
62. Wang, X. *et al.* Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors. *Phys. Rev. Lett.* **100,** 206803 (2008).
63. Akturk, A. & Goldsman, N. Electron transport and full-band electron-phonon interactions in graphene. *J. Appl. Phys.* **103,** 053702 (2008).
64. Shishir, R. S. & Ferry, D. K. Velocity saturation in intrinsic graphene. *J. Phys. Condens. Matter* **21,** 344201 (2009).
65. Barreiro, A., Lazzeri, M., Moser, J., Mauri, F. & Bachtold, A. Transport properties of graphene in the high-current limit. *Phys. Rev. Lett.* **103,** 076601 (2009).
66. Schroder, D. K. *Semiconductor Material and Device Characterization* (Wiley, 1990).
67. Fang, T., Konar, A., Xing, H. & Jena, D. Carrier statistics and quantum capacitance of graphene sheets and nanoribbons. *Appl. Phys. Lett.* **91,** 092109 (2007).
68. Chen, Z. & Appenzeller, J. in *Tech. Dig. IEDM 2008*, paper 21.1 (IEEE, 2008).
69. Meric, I., Baklitskaya, N., Kim, P. & Shepard, K. L. in *Tech. Dig. IEDM 2008*, paper 21.2 (IEEE, 2008).
70. Meric, I. *et al.* Current saturation in zero-bandgap, top-gated graphene field-effect transistors. *Nature Nanotech*. **3,** 654–659 (2008).
71. Kedzierski, J. *et al.* Graphene-on-insulator transistors made using C on Ni chemical-vapor deposition. *IEEE Electron Dev. Lett.* **30,** 745–747 (2009).
72. Li, X. *et al.* Large-area synthesis of high-quality and uniform graphene films on copper foils. *Science* **324,** 1312–1314 (2009).
73. Lin, Y-M. *et al.* 100-GHz transistors from wafer-scale epitaxial graphene. *Science* **327,** 662 (2010).
74. Moon, J. S. *et al.* Epitaxial-graphene RF field-effect transistors on Si-face 6H-SiC substrates. *IEEE Electron Dev. Lett.* **30,** 650–652 (2009).
75. Tahy, K. *et al.* in *Proc. Dev. Res. Conf. 2009* 207–208 (IEEE, 2009).
76. Thiele, S., Schaefer, J. A. & Schwierz, F. Modeling of graphene metal–oxide–semiconductor field-effect transistors with gapless large-area graphene channels. *J. Appl. Phys.* **107,** 094505 (2010).
77. Lin, Y-M. *et al.* Dual-gate graphene FETs with $f_T$ of 50 GHz. *IEEE Electron Dev. Lett.* **31,** 68–70 (2010).
78. Nougaret, N. *et al.* 80 GHz field-effect transistors produced using high purity semiconducting single-walled carbon nanotubes. *Appl. Phys. Lett.* **94,** 243505 (2009).
79. Rutherglen, C., Jain, D. & Burke, P. Nanotube electronics for radiofrequency applications. *Nature Nanotech.* **4,** 811–819 (2009).
80. Yoon, Y. & Guo, J. Effects of edge roughness in graphene nanoribbon transistors. *Appl. Phys. Lett.* **91,** 073103 (2007).
81. Basu, D., Gilbert, M. J., Register, L. F., Banerjee, S. K. & MacDonald, A. H. Effect of edge roughness on electronic transport in graphene nanoribbon channel metal–oxide–semiconductor field-effect transistors. *Appl. Phys. Lett.* **92,** 042114 (2008).
82. Liao, L. *et al.* Top-gated graphene nanoribbon transistors with ultrathin high-*k* dielectrics. *Nano Lett.* **10,** 1917–1921 (2010).
83. Xia, F., Farmer, D. B., Lin, Y-M. & Avouris, Ph. Graphene field-effect transistors with high on/off current ratio and large transport band gap at room temperature. *Nano Lett.* **10,** 715–718 (2010).
84. Iannaccone, G. *et al.* in *Tech. Dig. IEDM 2009* 245–248 (IEEE, 2009).
85. Nagashio, K., Nishimura, T., Kita, K. & Toriumi, A. in *Tech. Dig. IEDM 2009* 565–568 (IEEE, 2009).
86. Russo, S., Cracuin, M. F., Yamamoto, Y., Morpurgo, A. F. & Tarucha, S. Contact resistance in graphene-based devices. *Physica E* **42,** 677–679 (2010).
87. Huard, B., Stander, N., Sulpizio, J. A. & Goldhaber-Gordon, D. Evidence of the role of contacts on the observed electron-hole asymmetry in graphene. *Phys. Rev. B* **78,** 121402 (2008).
88. Boucart, K. & Ionescu, A. M. Double-gate tunnel FET with high-κ gate dielectric. *IEEE Trans. Electron. Dev.* **54,** 1725–1733 (2007).
89. Appenzeller, J., Lin, Y-M., Knoch, J. & Avouris, Ph. Band-to-band tunneling in carbon nanotube field-effect transistor. *Phys. Rev. Lett.* **93,** 196805 (2004).
90. Luisier, M. & Klimeck, G. in *Proc. Dev. Res. Conf. 2009* 201–202 (IEEE, 2009).
91. Fiori, G. & Iannaccone, G. Ultralow-voltage bilayer graphene tunnel FET. *IEEE Electron Dev. Lett.* **30,** 1096–1098 (2009).
92. Banerjee, S. K., Register, L. F., Tutuc, E., Reddy, D. & MacDonald, A. H. Bilayer pseudospin field-effect transistor (BiSFET): a proposed new logic device. *IEEE Electron Dev. Lett.* **30,** 158–160 (2009).
93. Murali, R., Brenner, K., Yang, Y., Beck, Th. & Meindl, J. D. Resistivity of graphene nanoribbon interconnects. *IEEE Electron Dev. Lett.* **30,** 611–613 (2009).
94. Awano, Y. in *Tech. Dig. IEDM 2009* 233–236 (IEEE, 2009).
95. Moser, J., Barreiro, A. & Bachtold, A. Current-induced cleaning of graphene. *Appl. Phys. Lett.* **91,** 163513 (2007).
96. Balandin, A. A. *et al.* Superior thermal conductivity of single-layer graphene. *Nano Lett.* **8,** 902–907 (2008).
97. Ferry, D. K., Gilbert, M. J. & Akis, R. Some considerations on nanowires in nanoelectronics. *IEEE Trans. Electron. Dev.* **55,** 2820–2826 (2008).
98. Iijima, S. Helical microtubules of graphitic carbon. *Nature* **354,** 56–58 (1991).
99. Tans, S. J., Verschueren, A. R. M. & Dekker, C. Room-temperature transistor based on a single carbon nanotube. *Nature* **393,** 49–52 (1998).
100. Li, S., Yu, Z., Yen, S-F., Tang, W. C. & Burke, P. J. Carbon nanotube transistor operation at 2.6 GHz. *Nano Lett.* **4,** 753–756 (2004).
101. Lee, S. *et al.* in *Tech. Dig. IEDM 2007* 255–258 (IEEE, 2007).
102. Nguyen, L. D., Tasker, P. J., Radulescu, D. C. & Eastman, L. F. Characterization of ultra-high-speed AlGaAs/InGaAs (on GaAs) MODFETs. *IEEE Trans. Electron. Dev.* **36,** 2243–2248 (1989).



## Acknowledgements

This work was financially supported by the 2008–2009 Excellence Research Grant of Technische Universität Ilmenau. The author thanks A. Castro Neto, K. Novoselov and Th. Seyller for discussions. He also thanks St. Thiele for his comments and for graphene MOSFET simulations, and M. Schlechtweg for providing GaAs metamorphic-HEMT data before publication.


## Additional information

The authors declare no competing financial interests.



© 2010 Macmillan Publishers Limited. All rights reserved